

FIG. 1

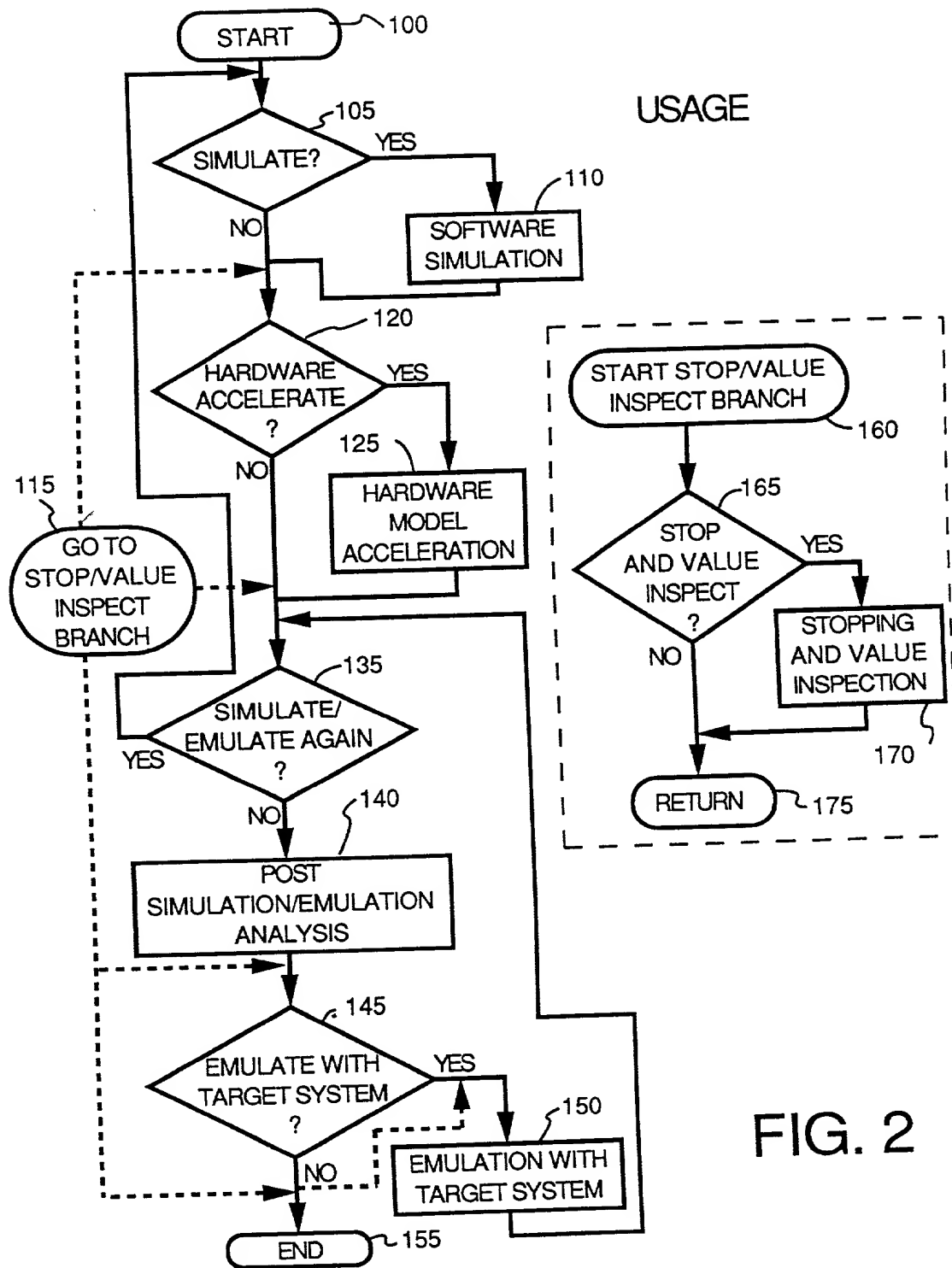


FIG. 2

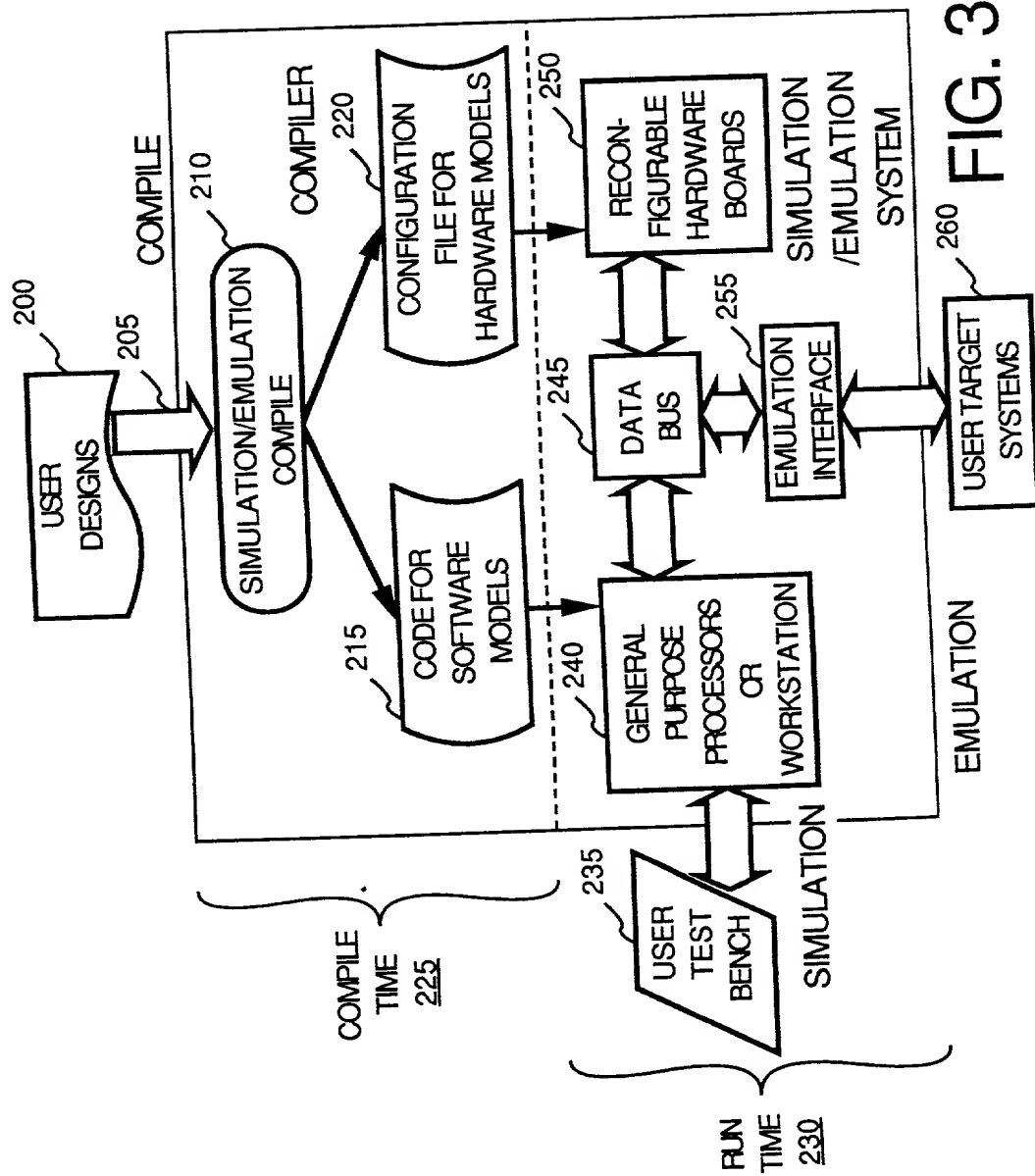


FIG. 3

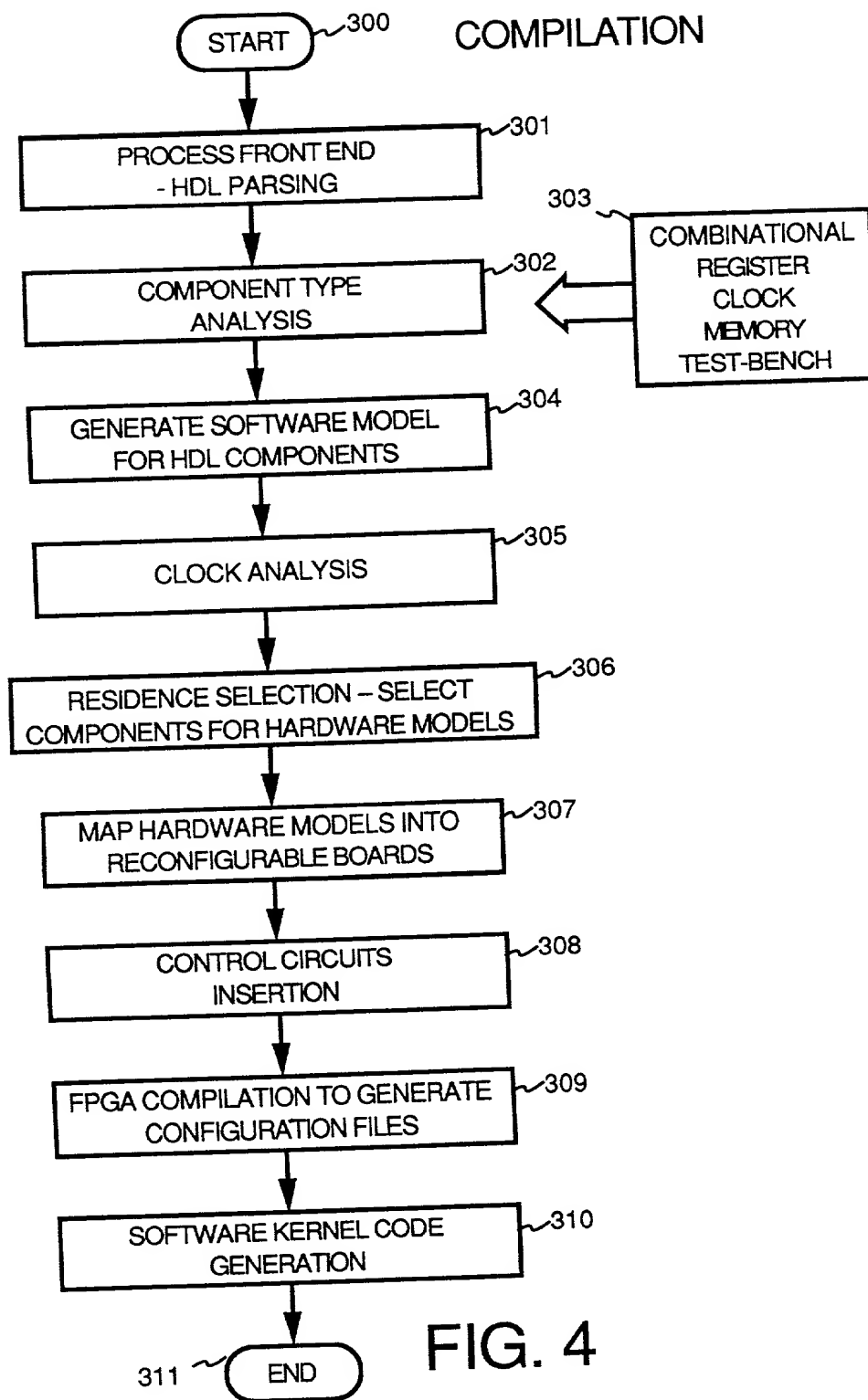


FIG. 4

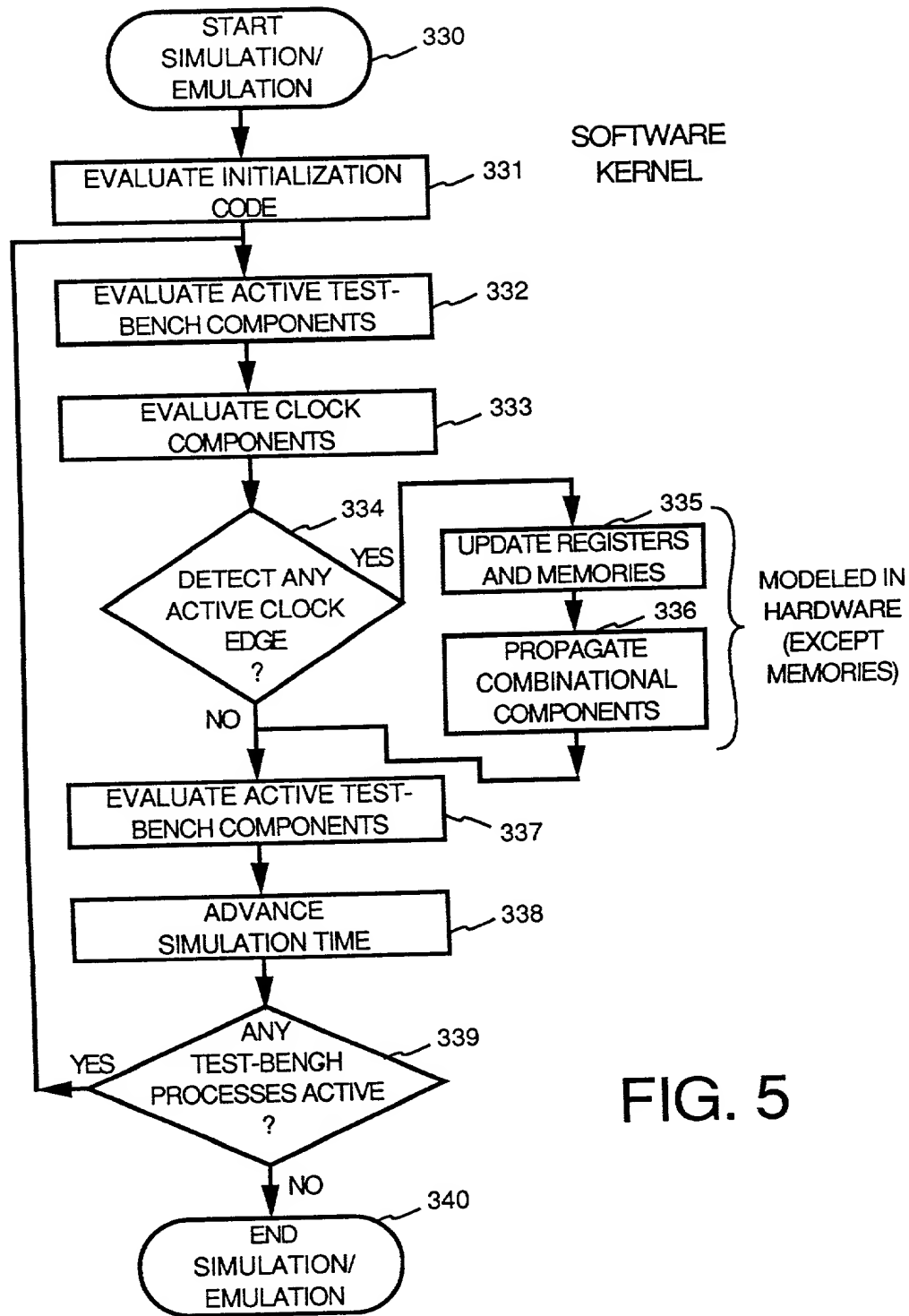


FIG. 5

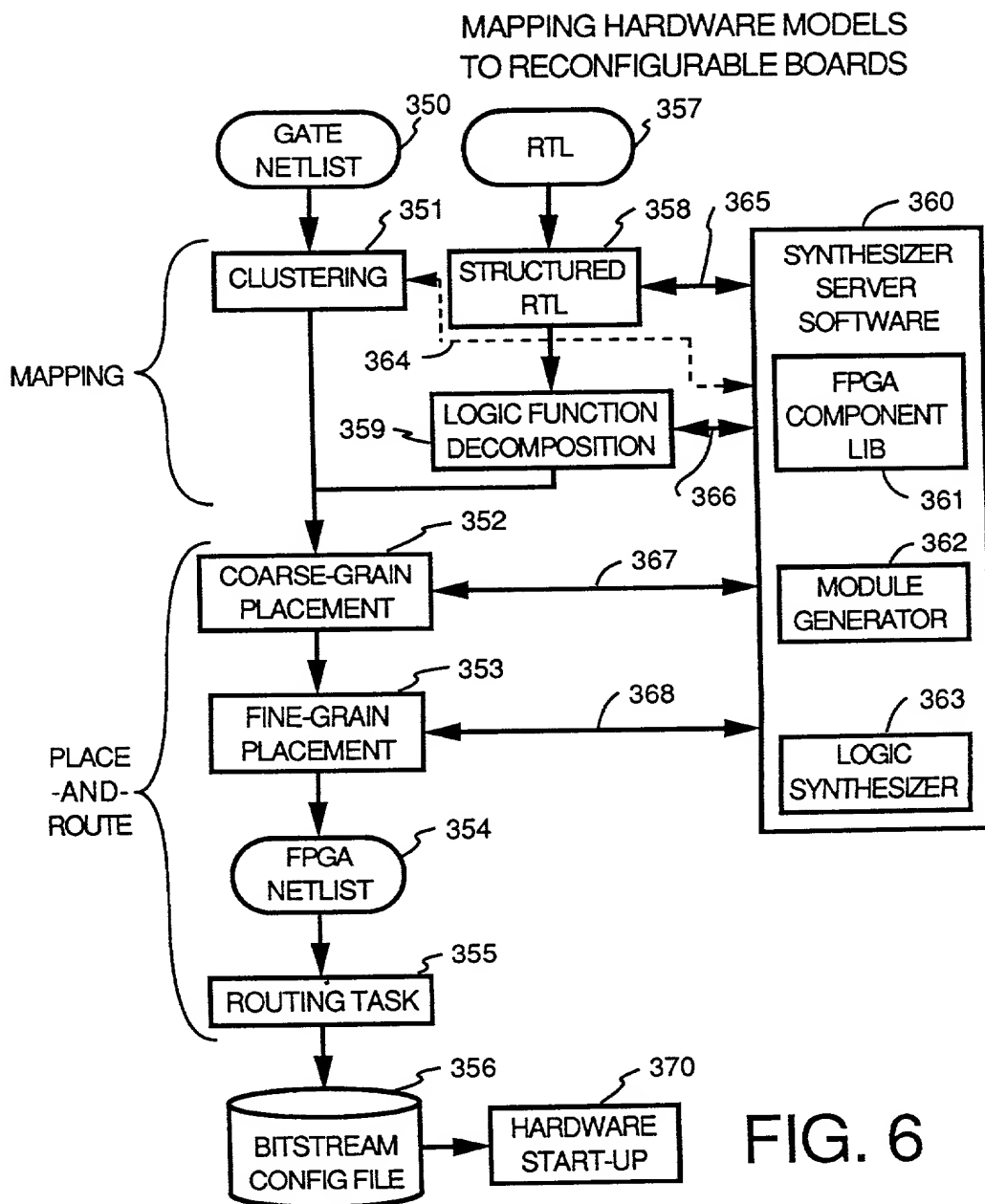


FIG. 6

	F11	F12	F13	F14	F21	F22	F23	F24	F31	F32	F33	F34	F41	F42	F43	F44
F11	1	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0
F12	1	1	1	1	0	1	0	0	0	1	0	0	0	1	0	0
F13	1	1	1	1	0	0	1	0	0	0	1	0	0	0	1	0
F14	1	1	1	1	0	0	0	1	0	0	0	1	0	0	0	1
F21	1	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0
F22	0	1	0	0	1	1	1	1	0	1	0	0	0	1	0	0
F23	0	0	1	0	1	1	1	1	0	0	1	0	0	0	1	0
F24	0	0	0	1	1	1	1	1	0	0	0	1	0	0	0	1
F31	1	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0
F32	0	1	0	0	0	1	0	0	1	1	1	1	0	1	0	0
F33	0	0	1	0	0	0	1	0	1	1	1	1	0	0	1	0
F34	0	0	0	1	0	0	0	1	1	1	1	1	0	0	0	1
F41	1	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1
F42	0	1	0	0	0	1	0	0	0	1	0	0	1	1	1	1
F43	0	0	1	0	0	0	1	0	0	0	1	0	1	1	1	1
F44	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	1

FIG. 7

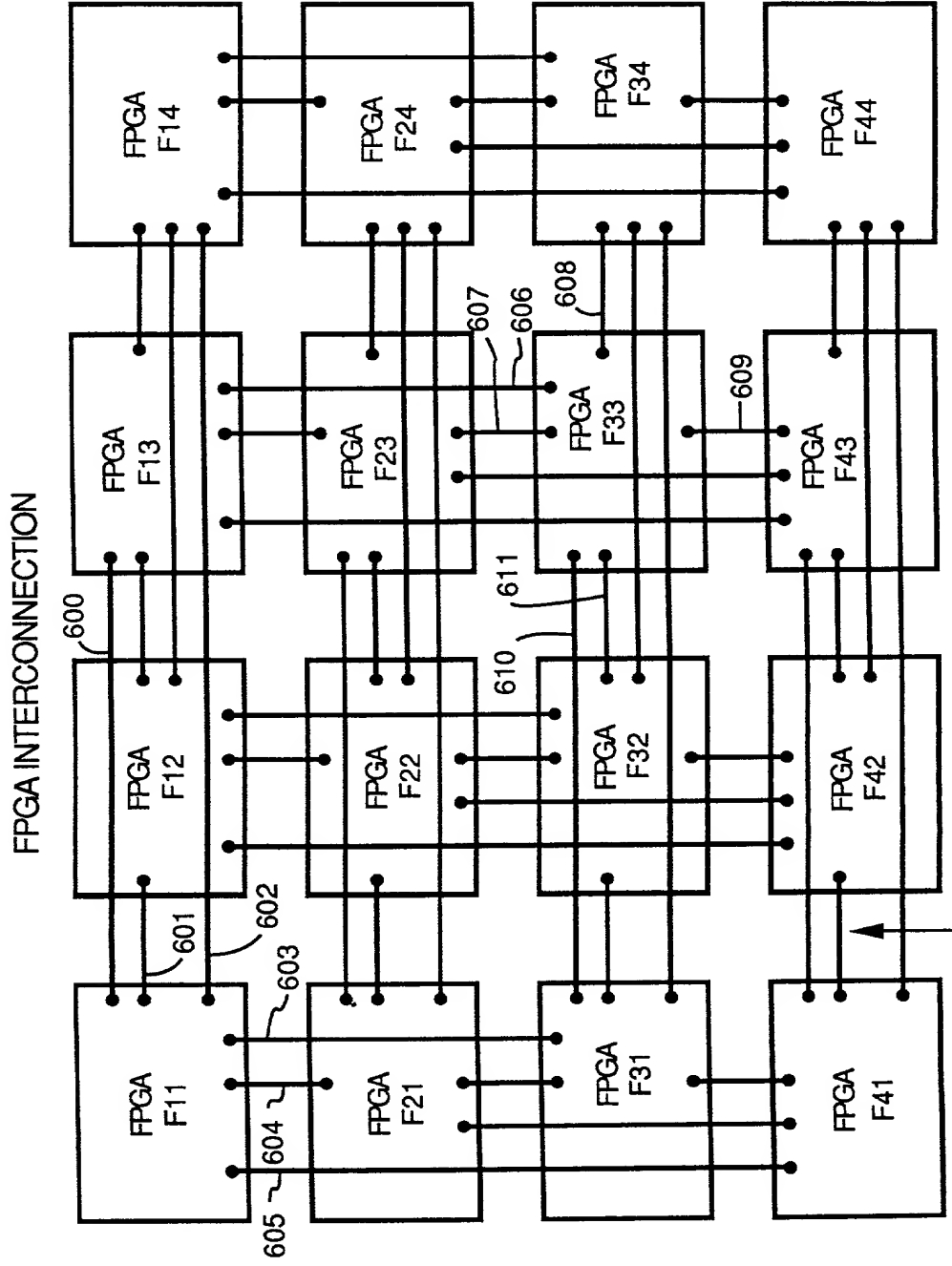


FIG. 8

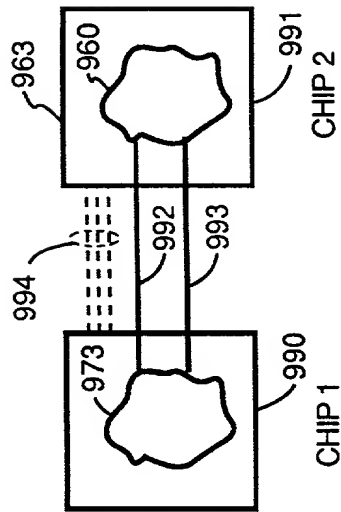


FIG. 9(a)

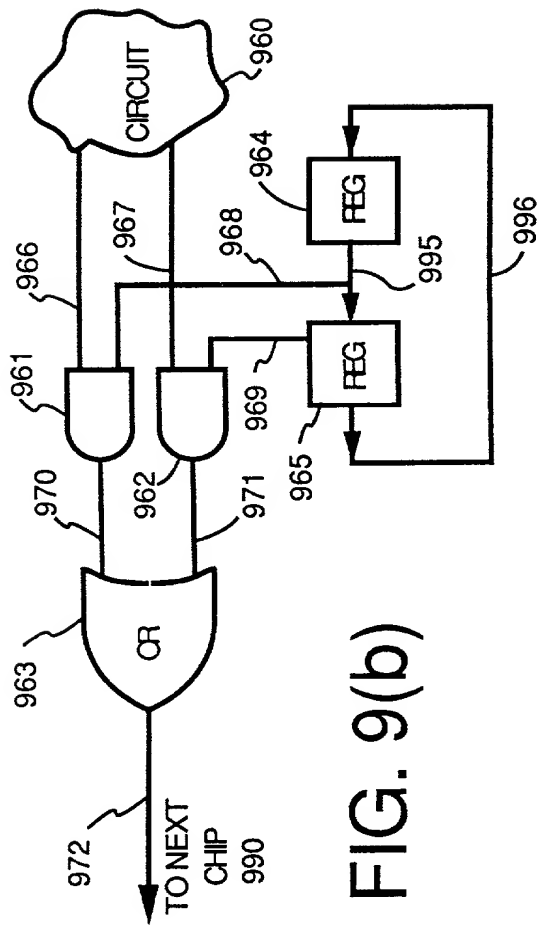


FIG. 9(b)

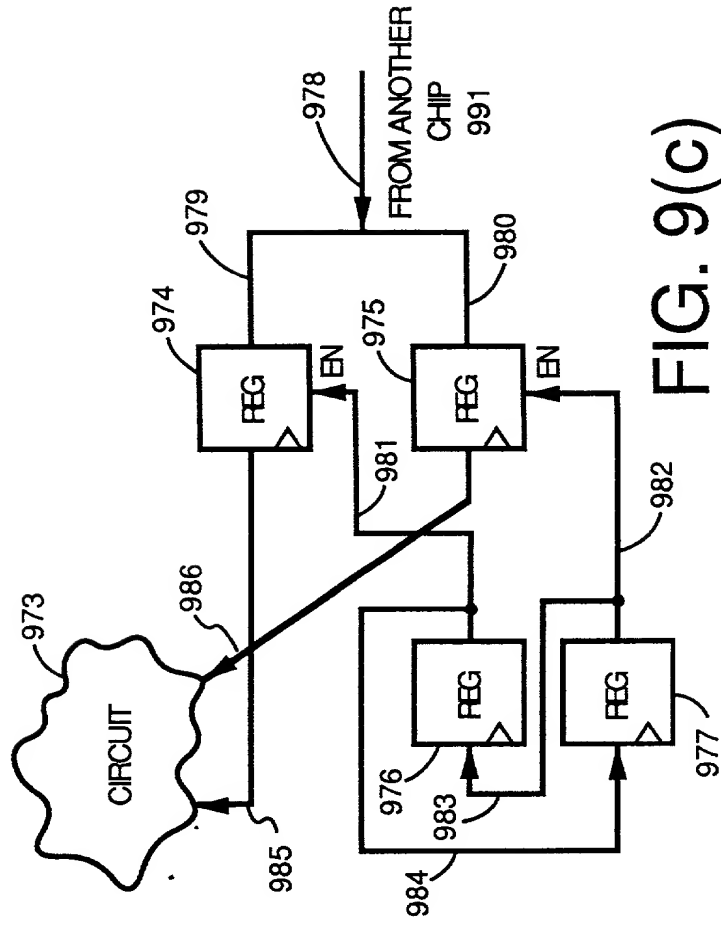


FIG. 9(c)

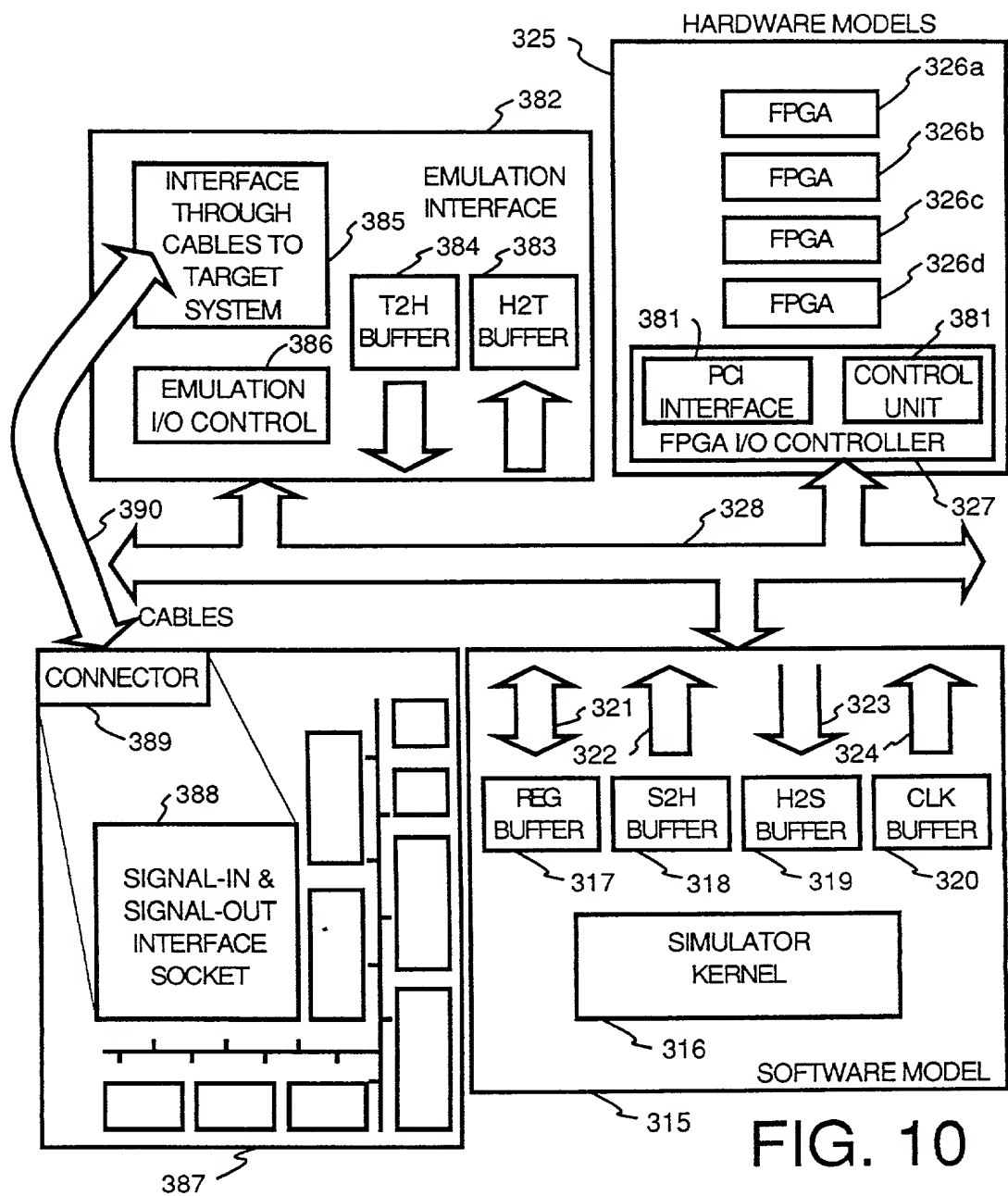


FIG. 10

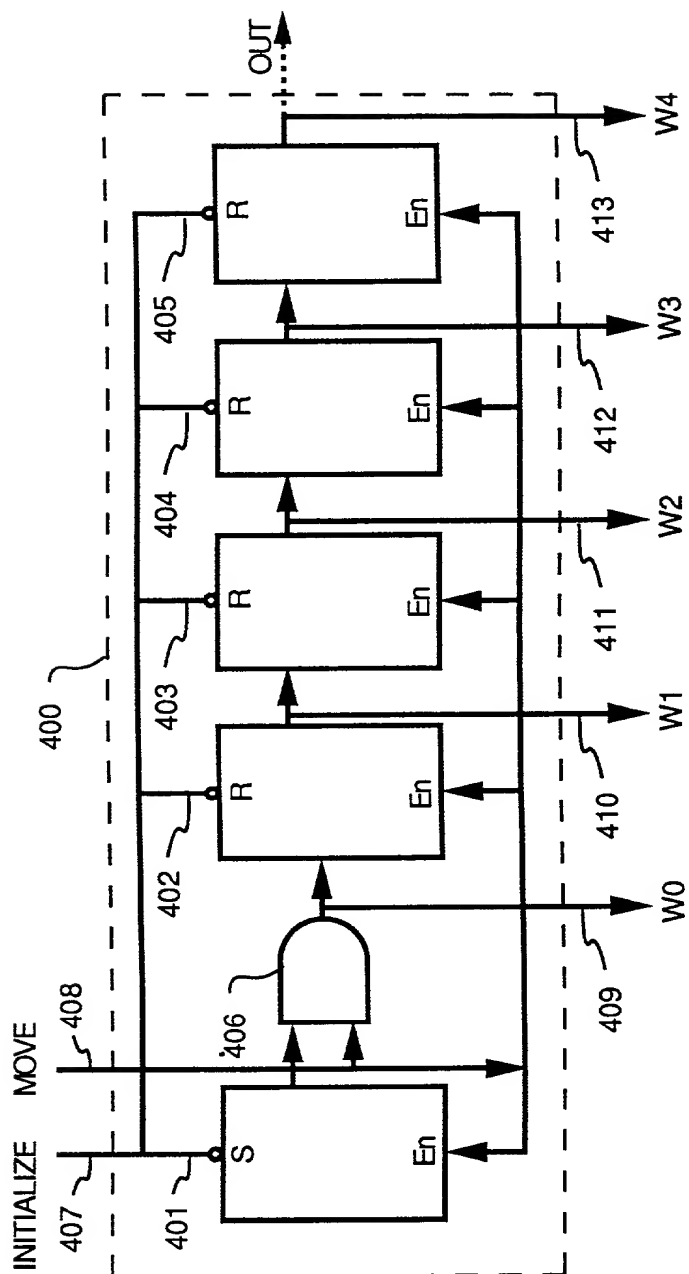


FIG. 11

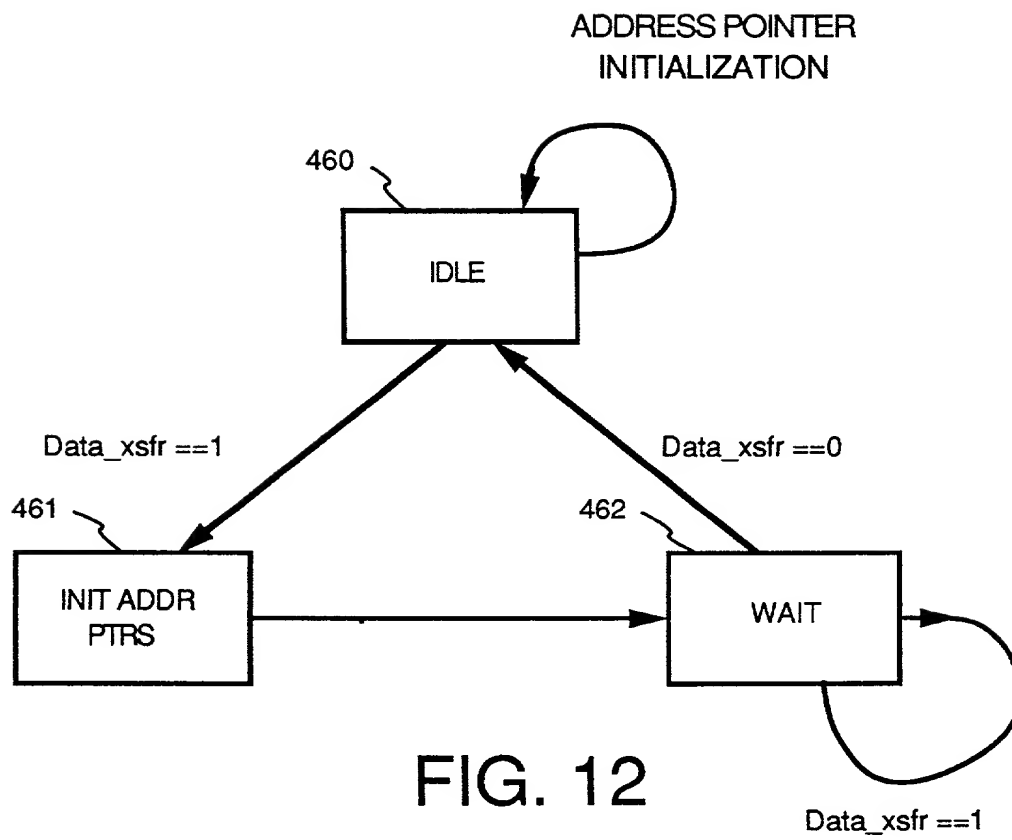


FIG. 12

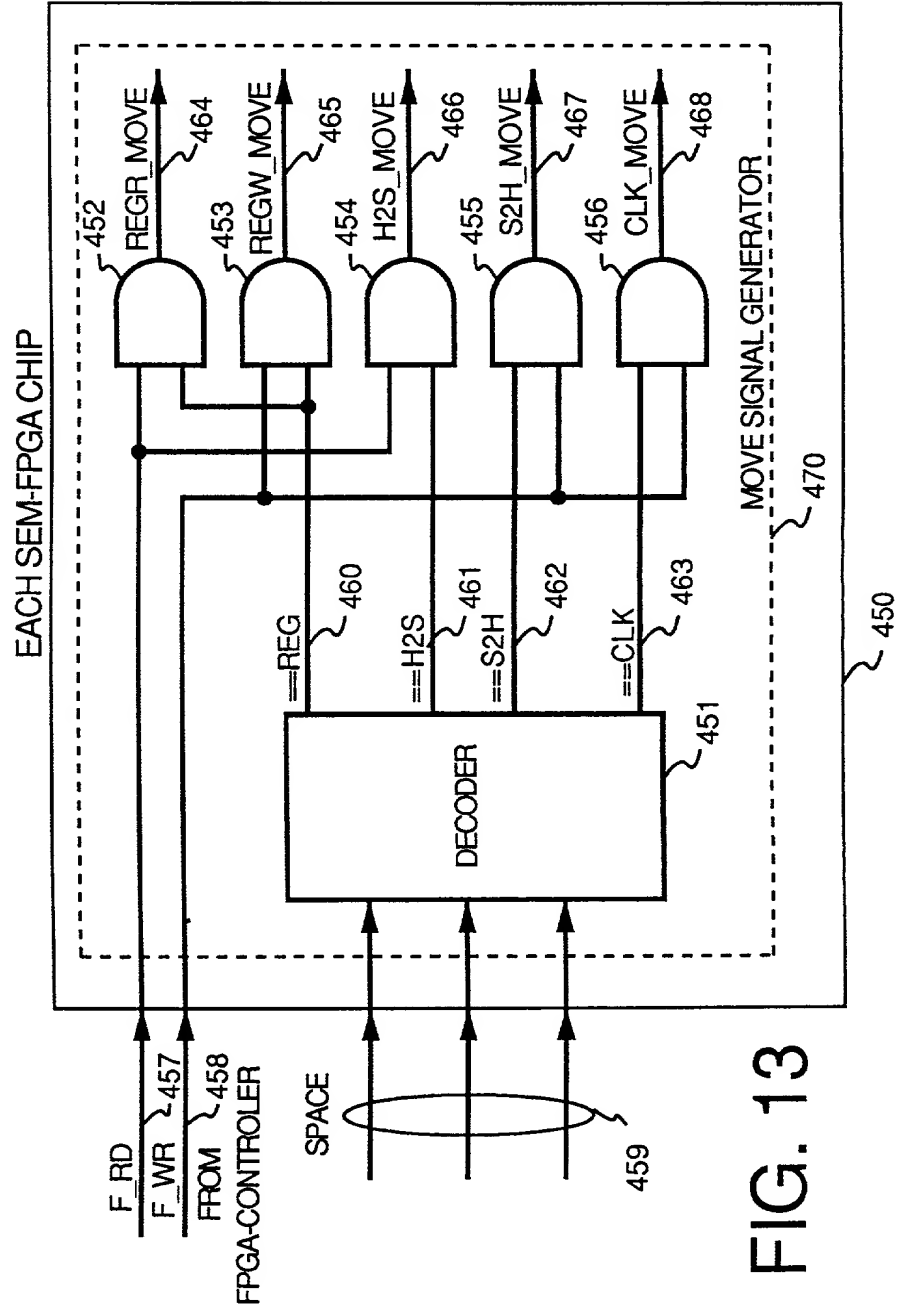
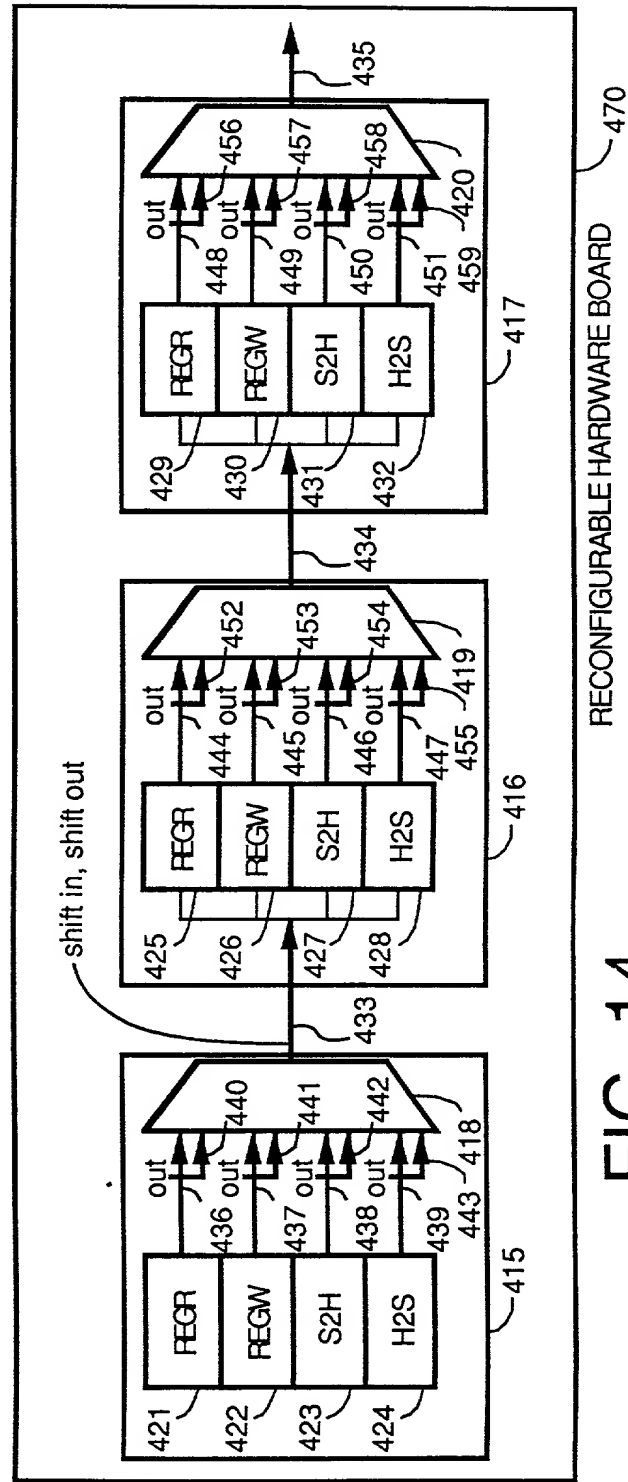
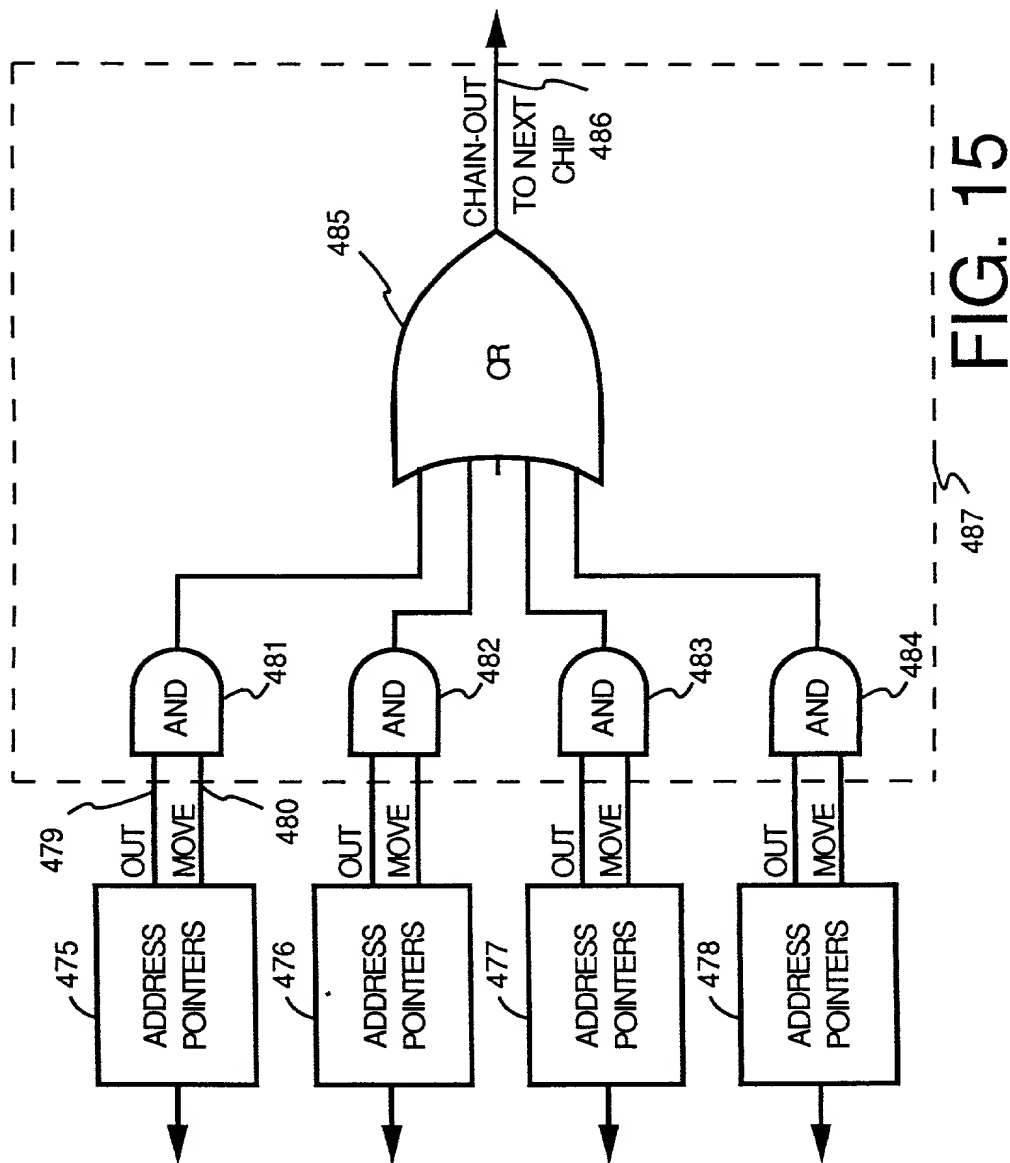


FIG. 13





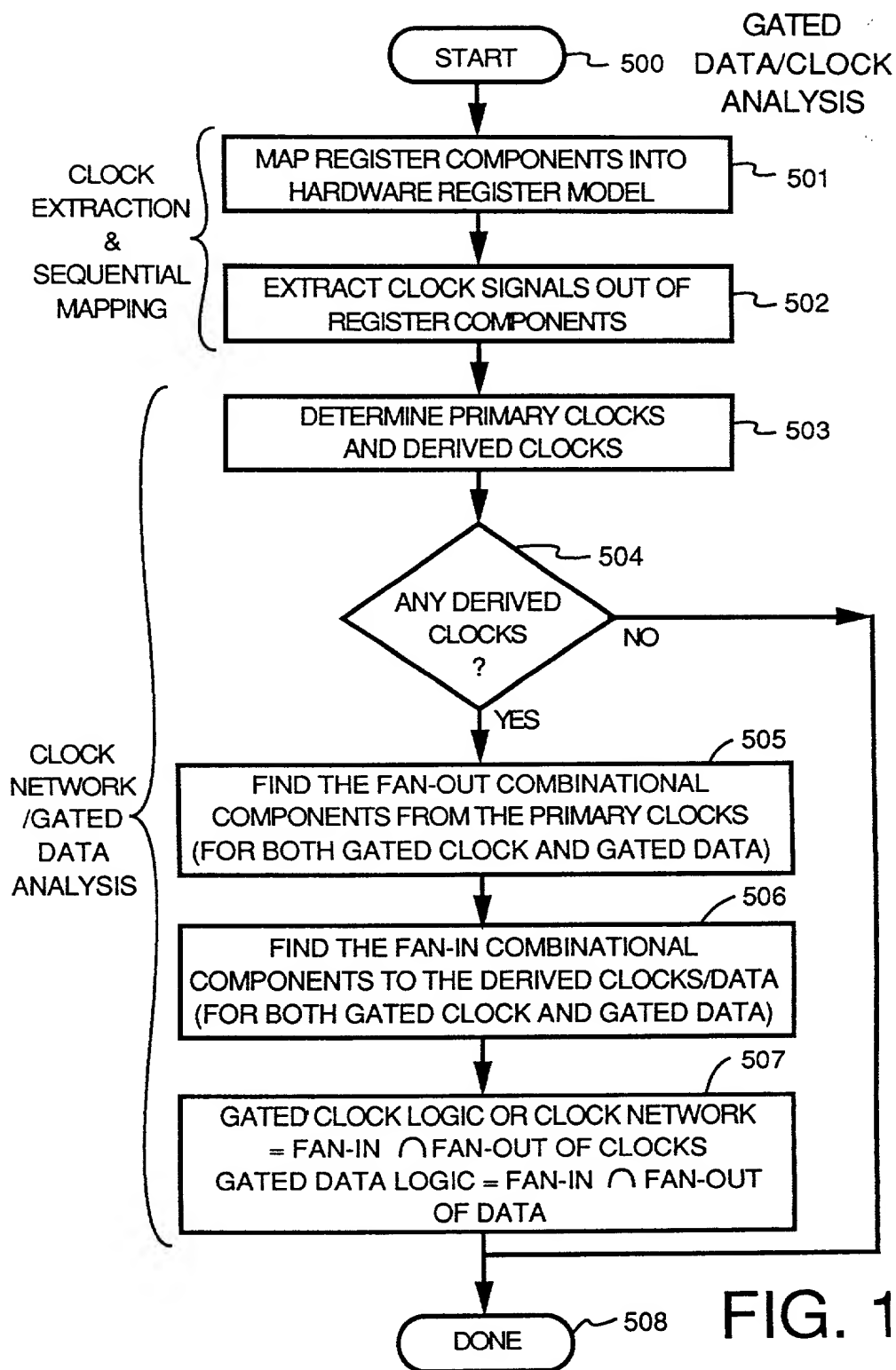


FIG. 16

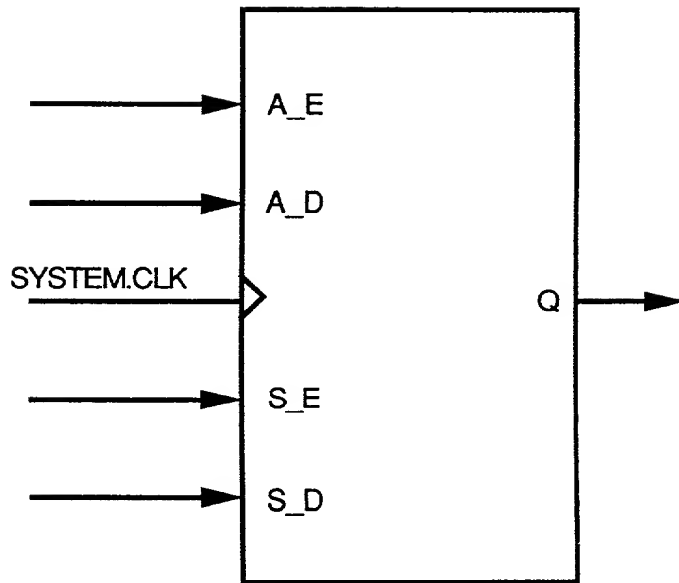


FIG. 17

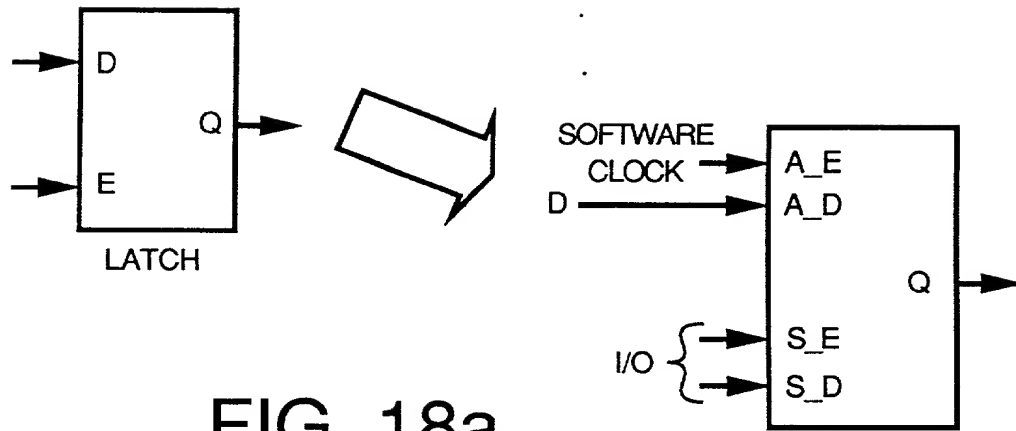


FIG. 18a

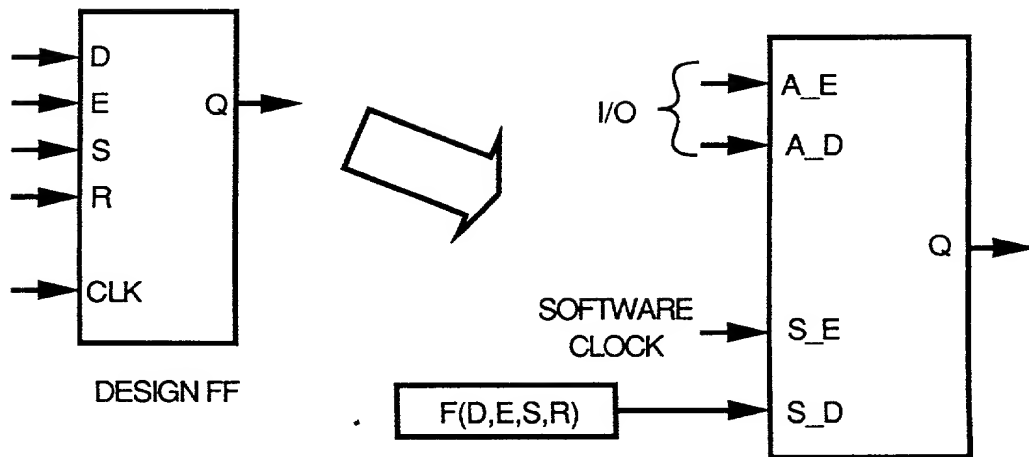


FIG. 18b

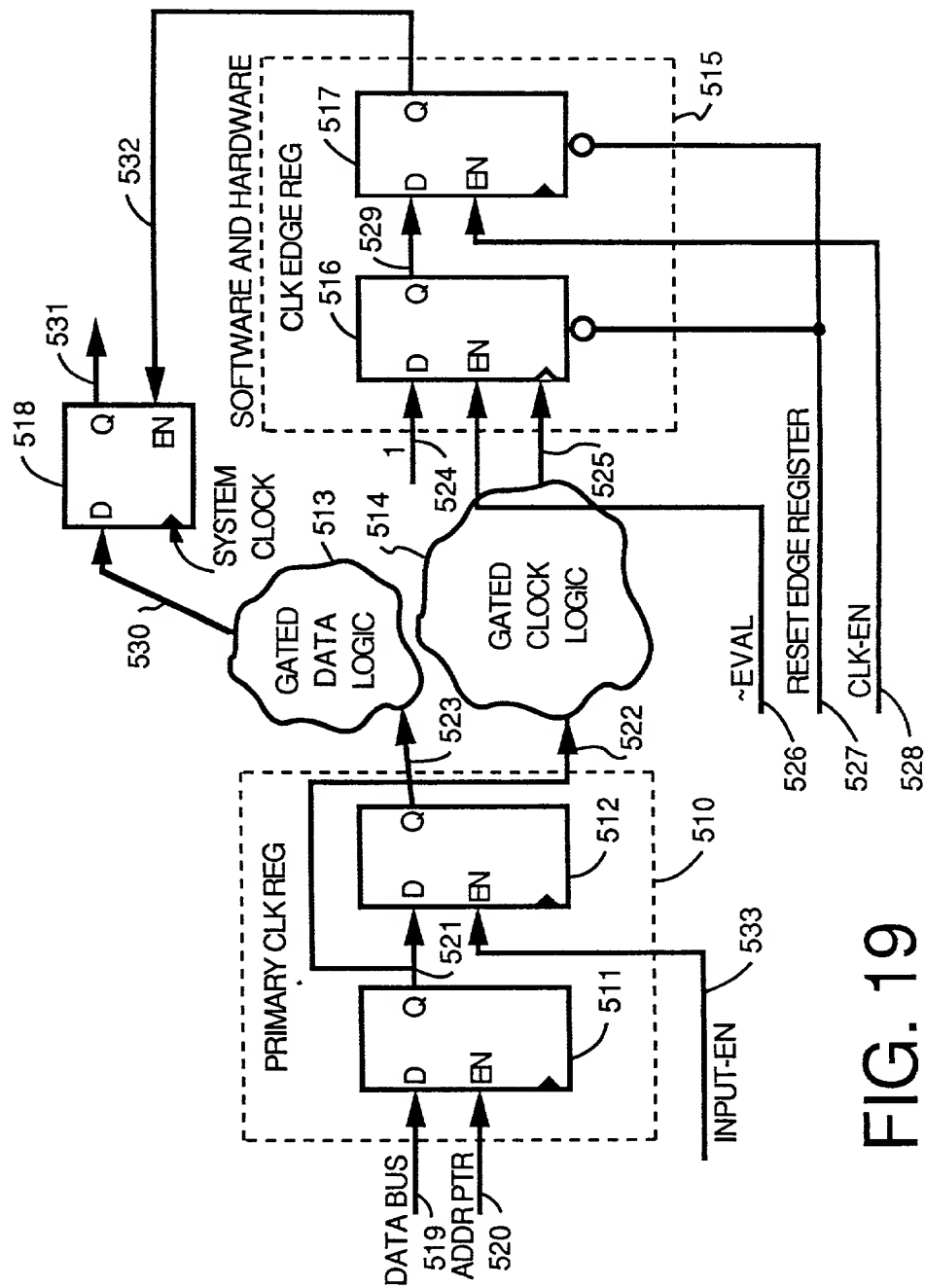


FIG. 19

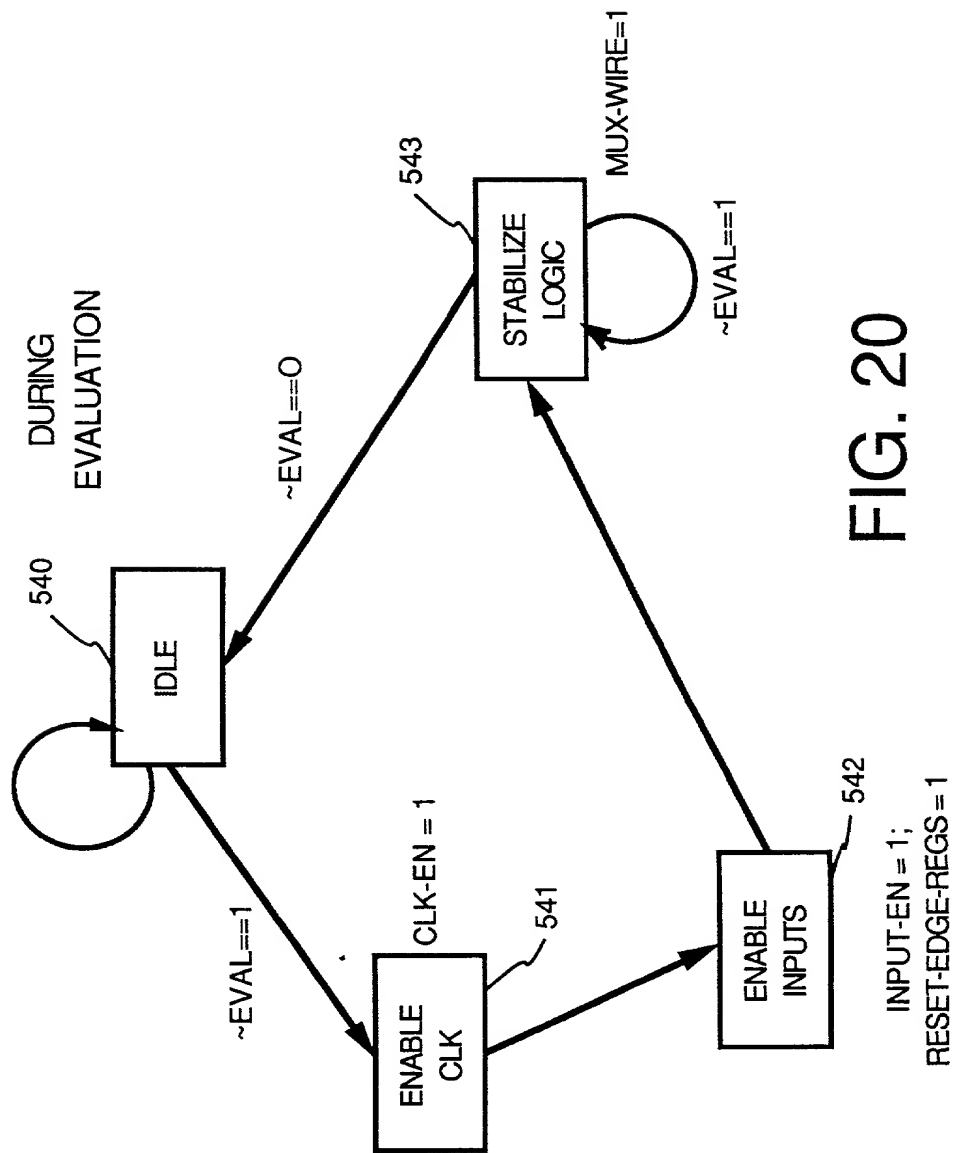


FIG. 20

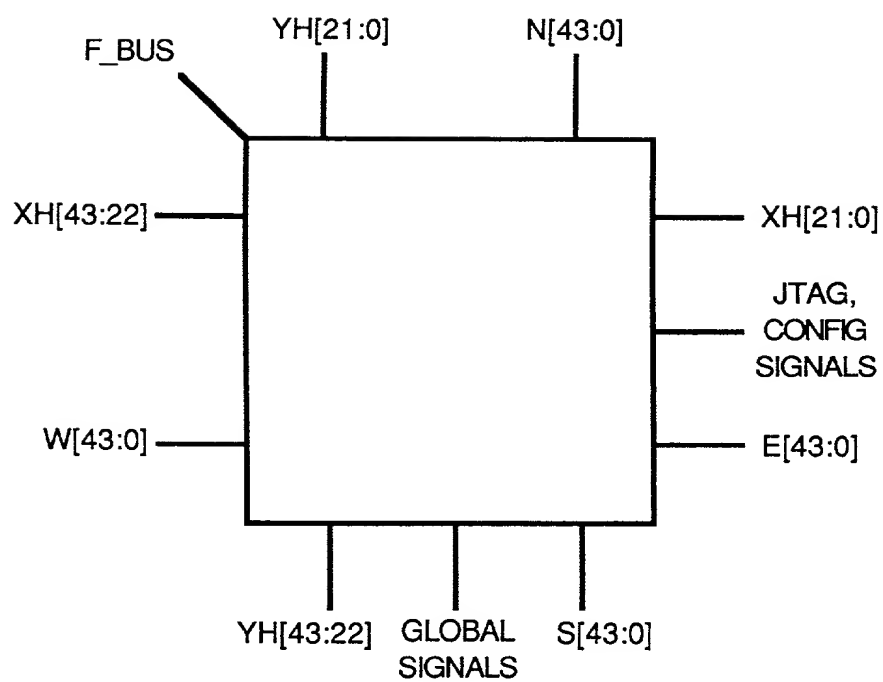


FIG. 21

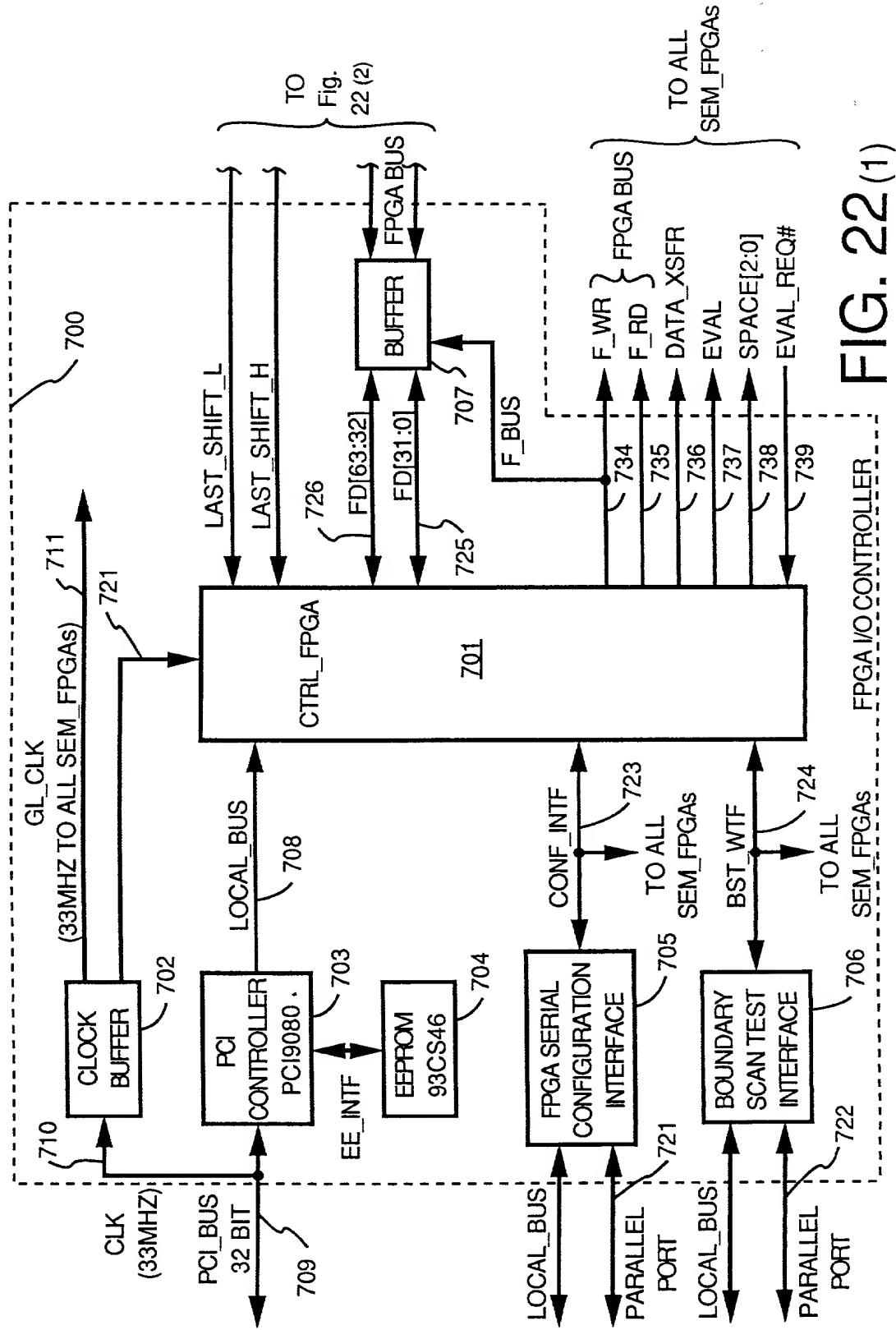


FIG. 22(1)

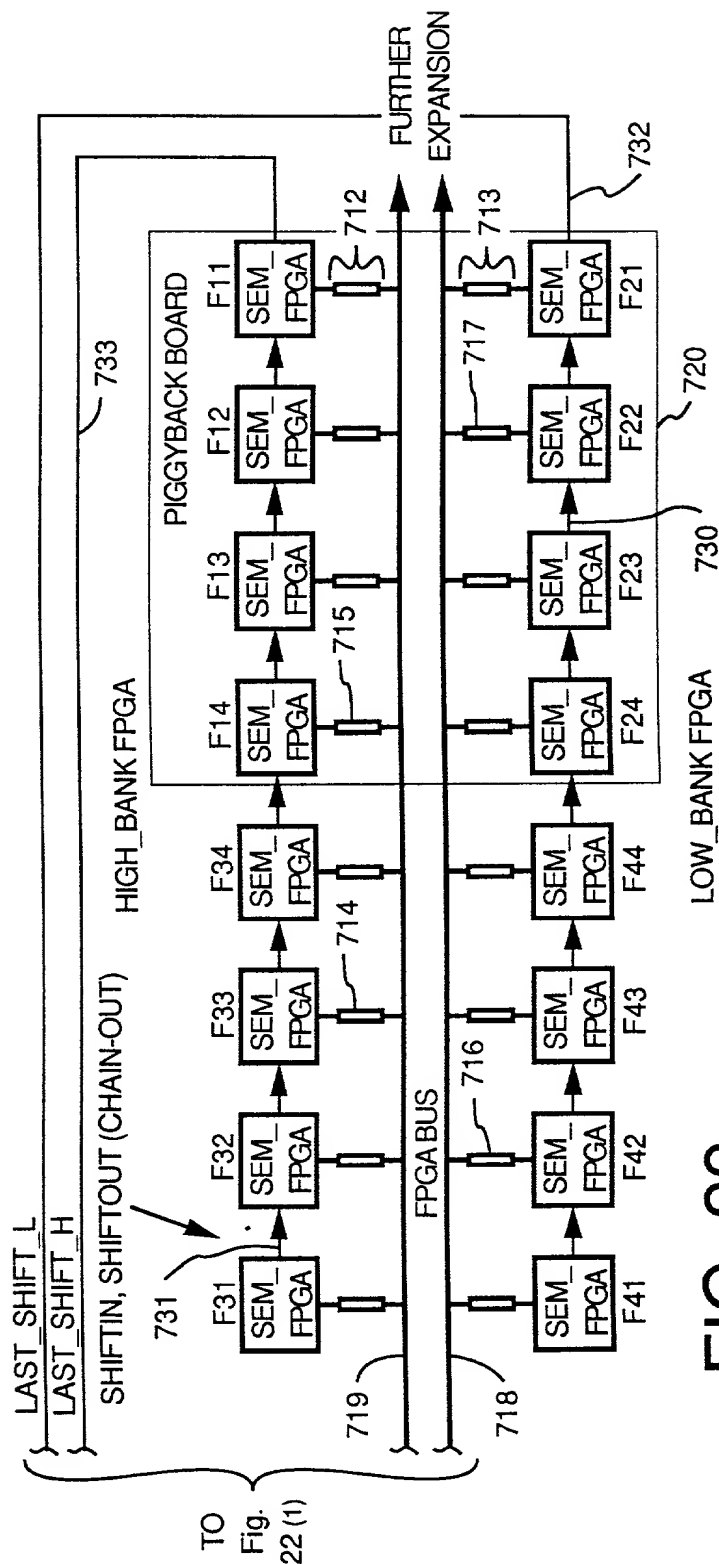


FIG. 22(2)

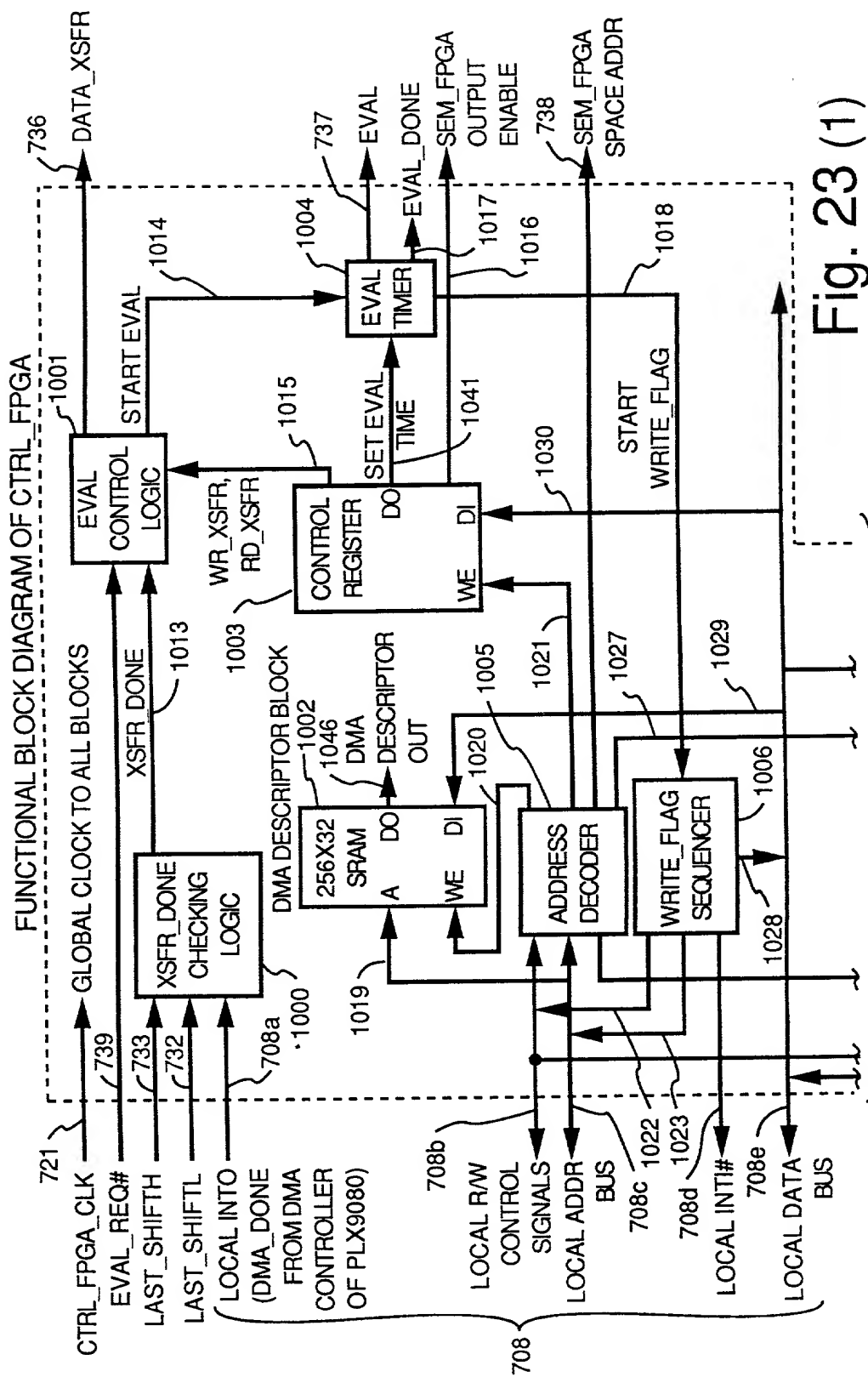


Fig. 23 (1)

To Fig. 23 (2)

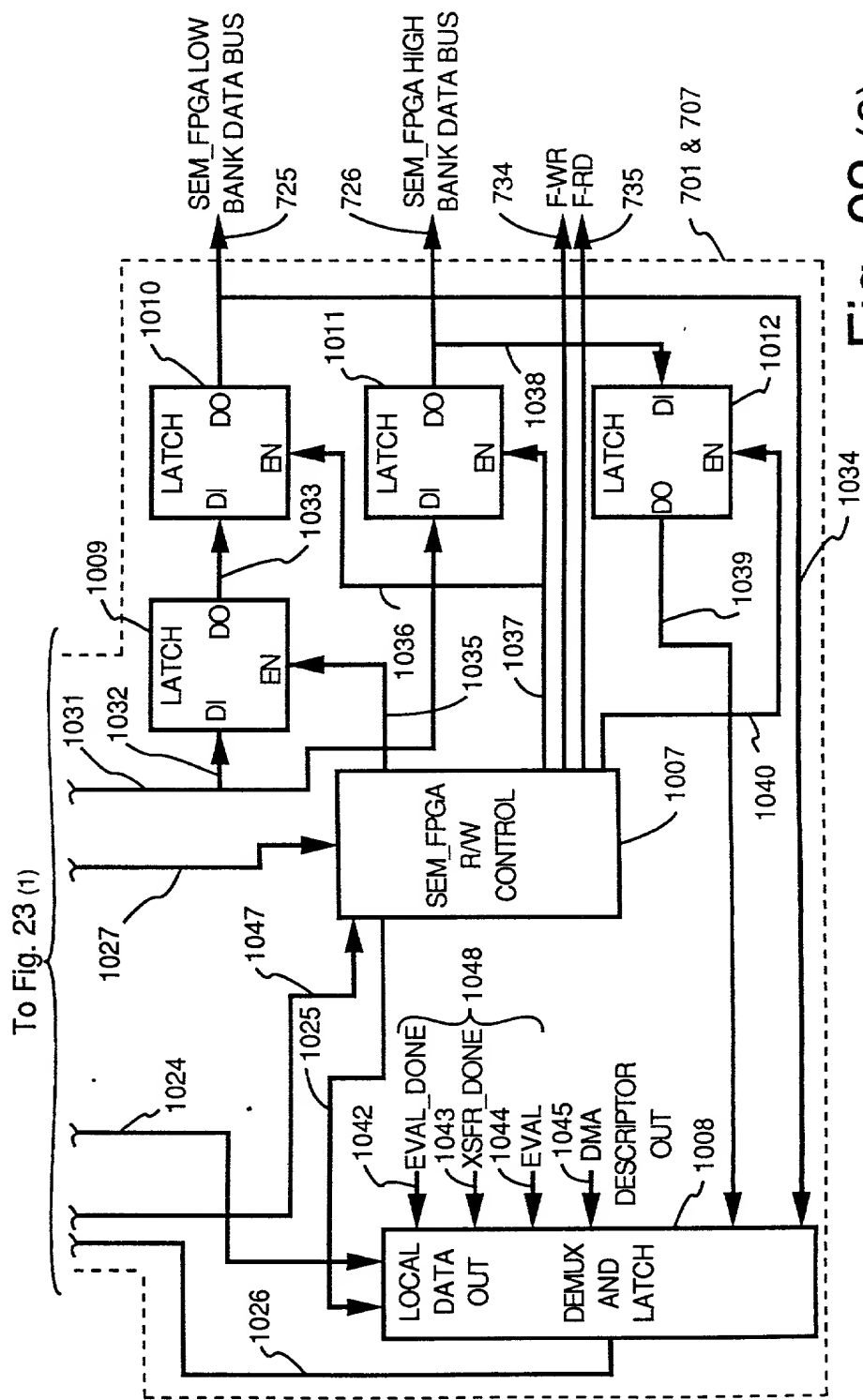


Fig. 23 (2)

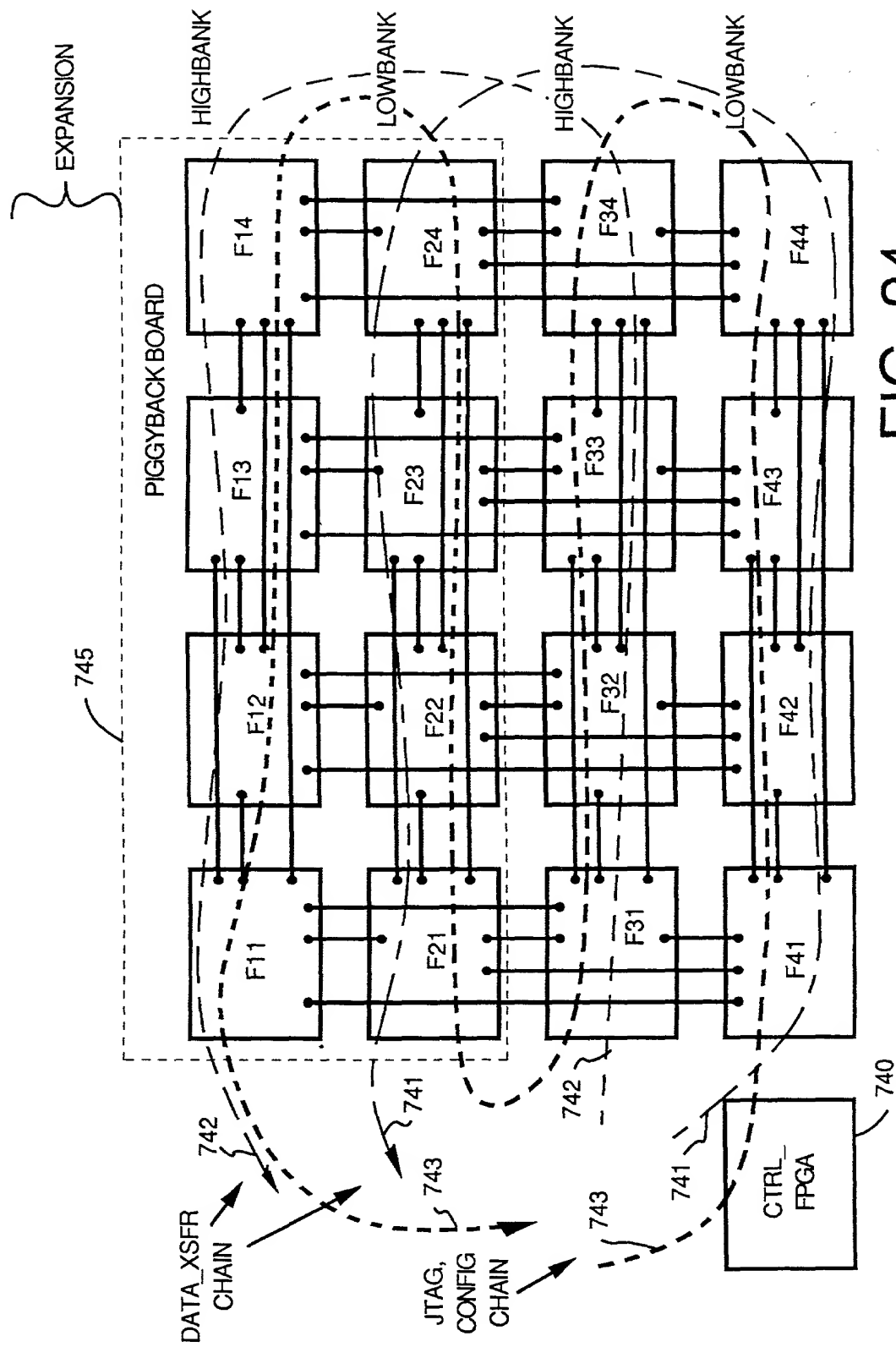


FIG. 24

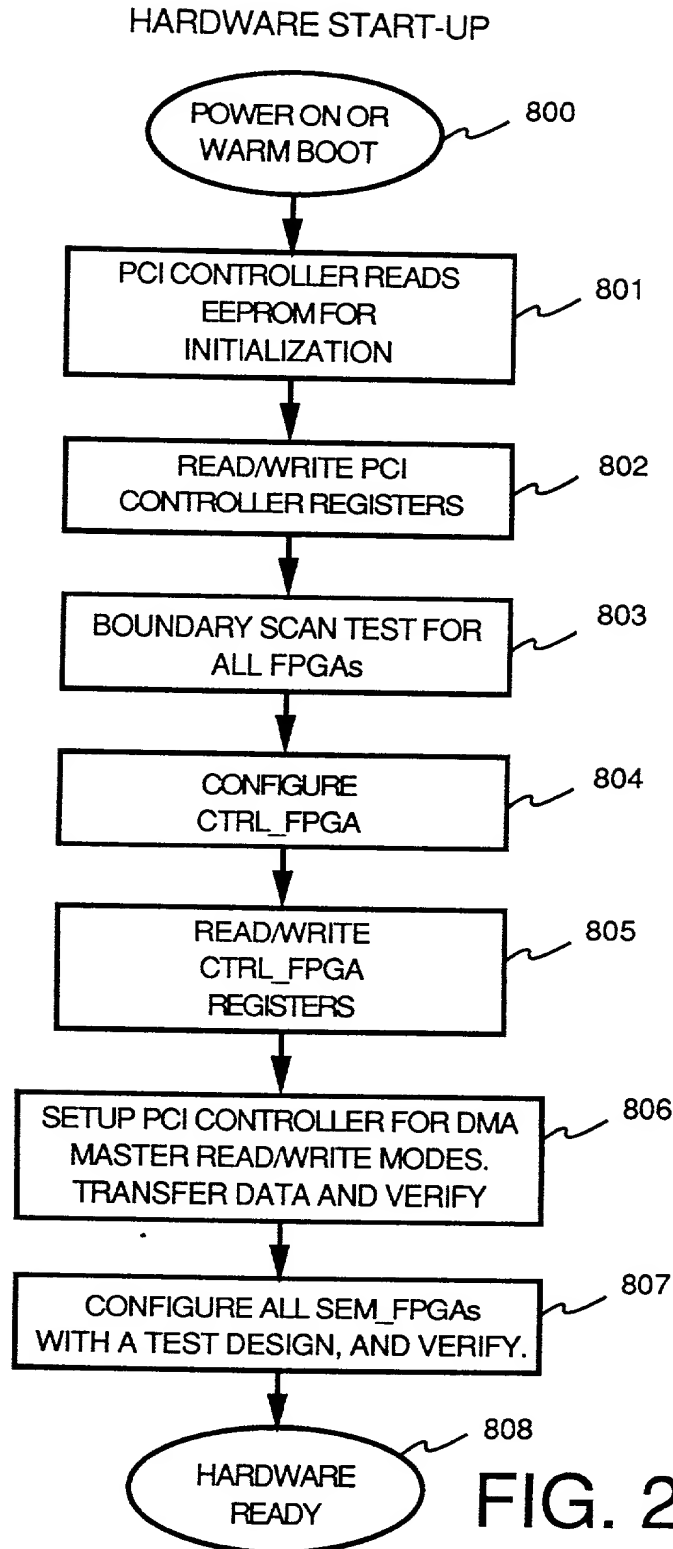


FIG. 25

```

module register (clock, reset, d, q);
input clock, d, reset;
output q;
reg q;

always@(posedge clock or negedge reset)
    if(~reset)
        q = 0;
    else
        q = d;
endmodule

module example;
    wire d1, d2, d3;
    wire q1, q2, q3;
    reg signin;
    wire sigout;
    reg clk, reset;

    register reg1 (clk, reset, d1, q1);
    register reg2 (clk, reset, d2, q2);
    register reg3 (clk, reset, d3, q3);

    assign d1 = signin ^ q3;
    assign d2 = q1 ^ q3;
    assign d3 = q2 ^ q3;
    assign sigout = q3;

    // a clock generator
    always
    begin
        clk = 0;
        #5;
        clk = 1;
        #5;
    end

    // a signal generator
    always
    begin
        #10;
        signin = $random;
    end

    // initialization
    initial
    begin
        reset = 0;
        signin = 0;
        #1;
        reset = 1;
        #5;
        $monitor($time, " %b, %b", signin, sigout);
        #1000 $finish;
    end
end module

```

Fig. 26

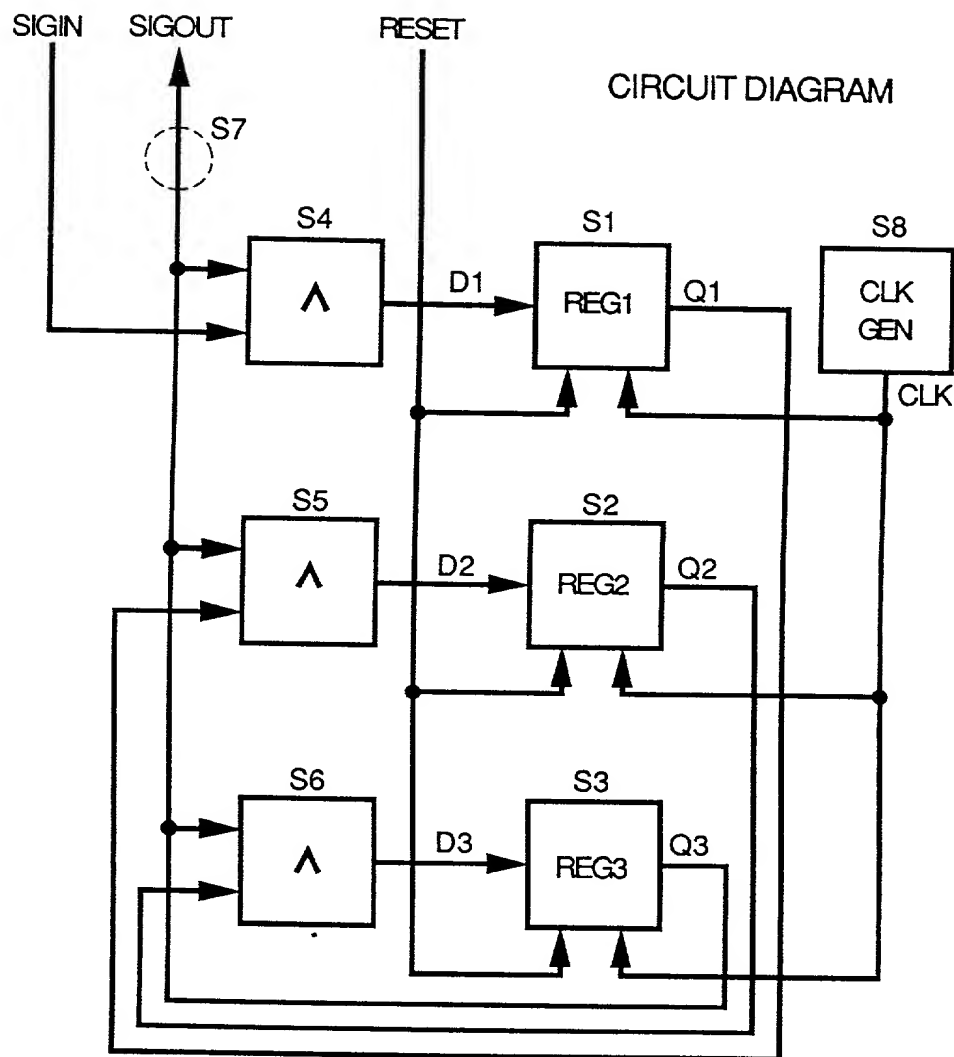


FIG. 27

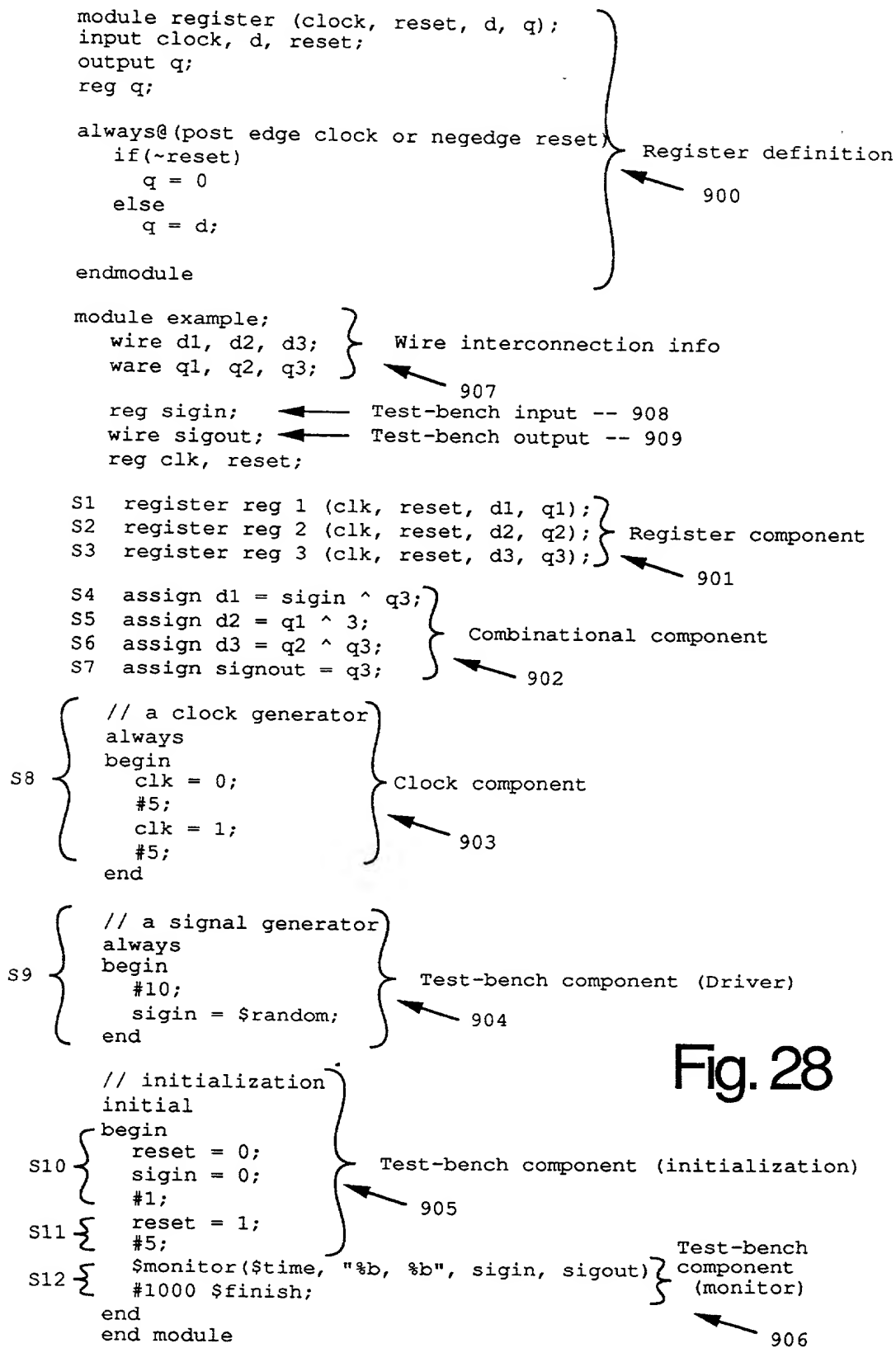


Fig. 28

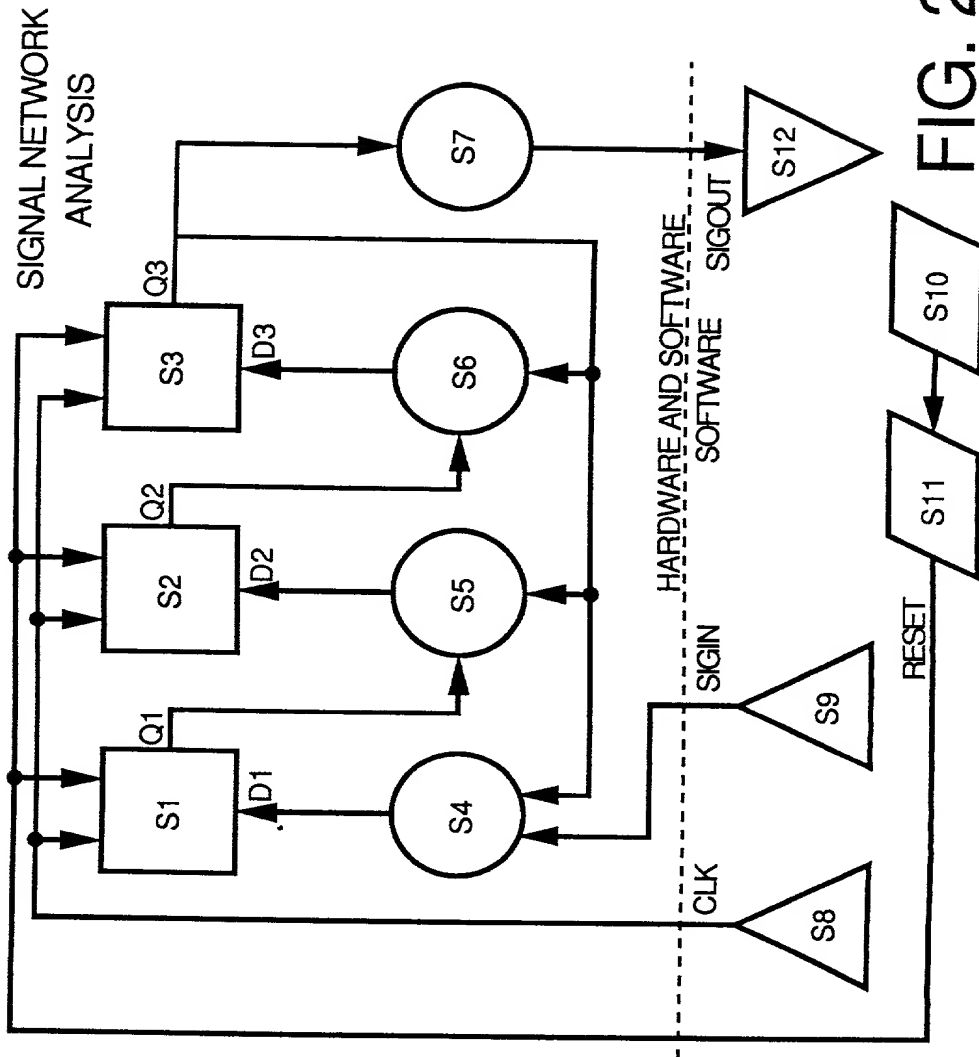


FIG. 29

FIG. 30

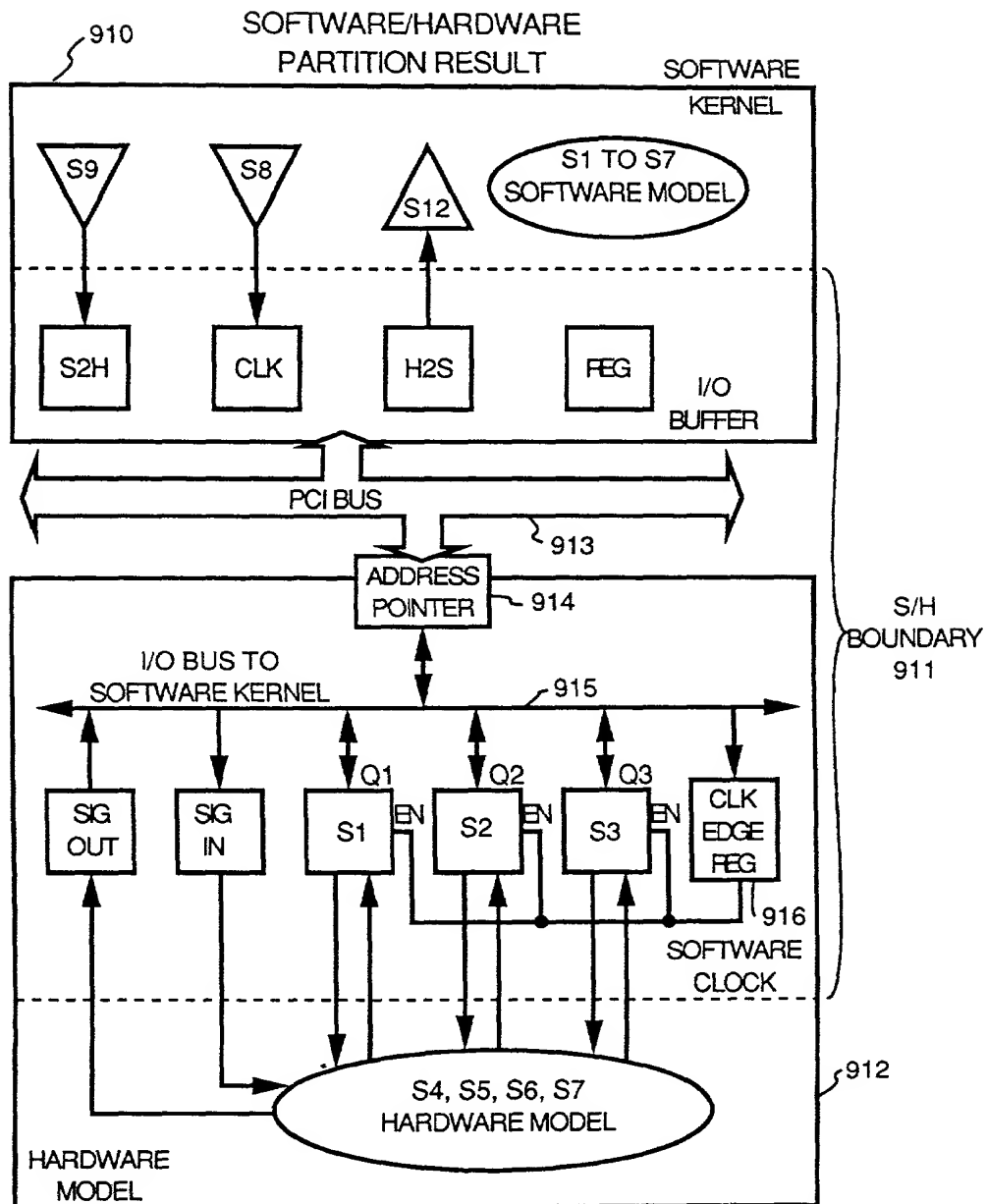


FIG. 30

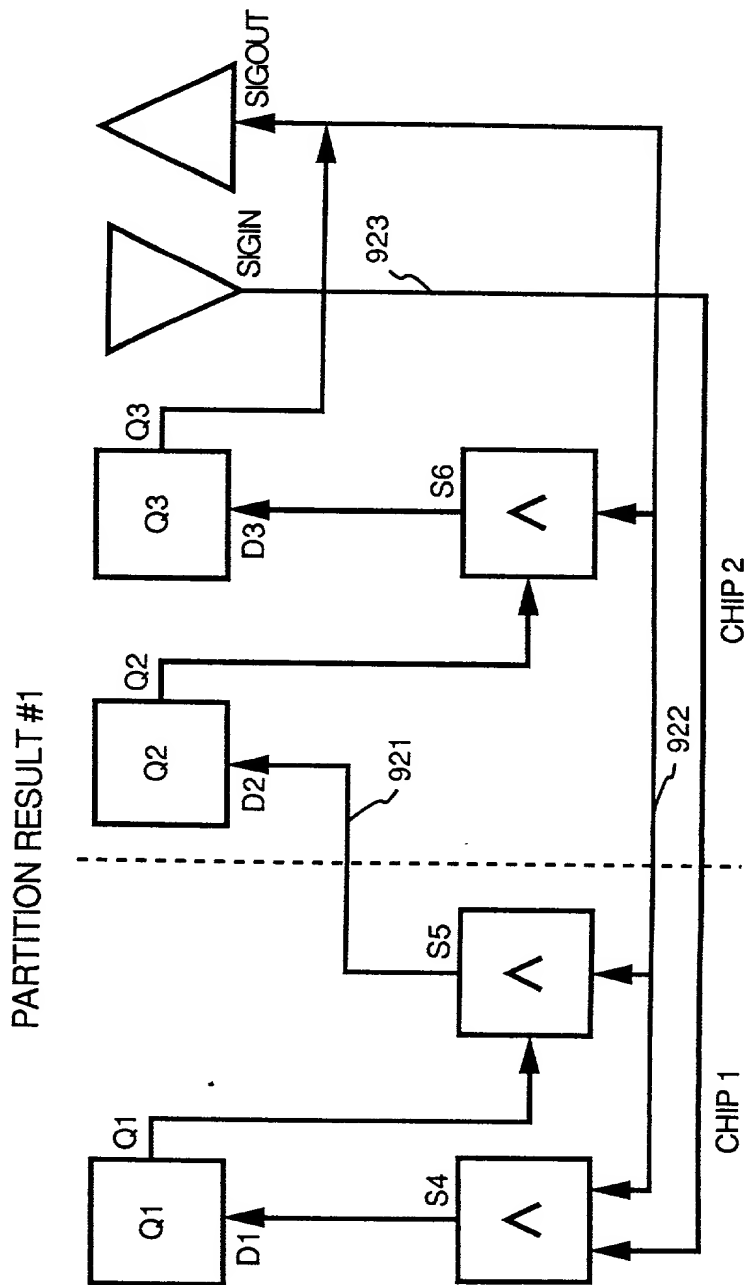
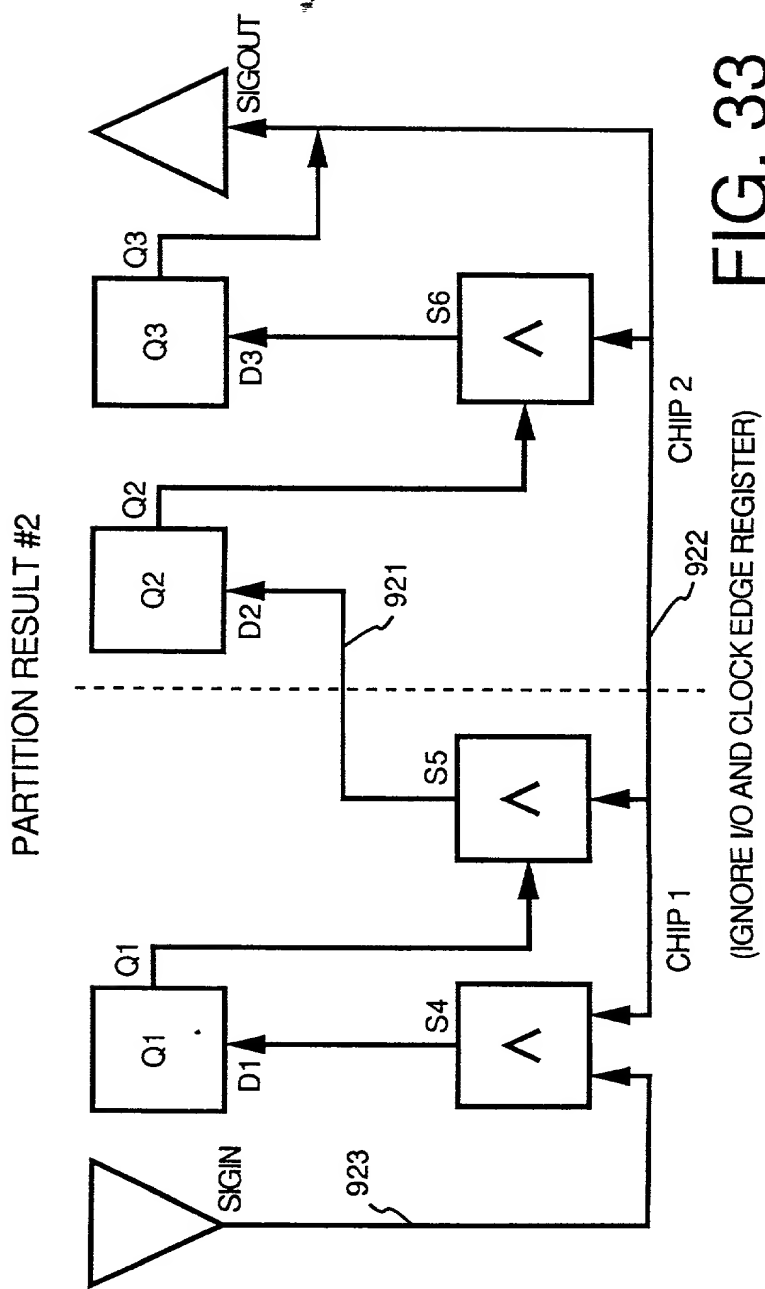


FIG. 32

(IGNORE I/O AND CLOCK EDGE REGISTER)



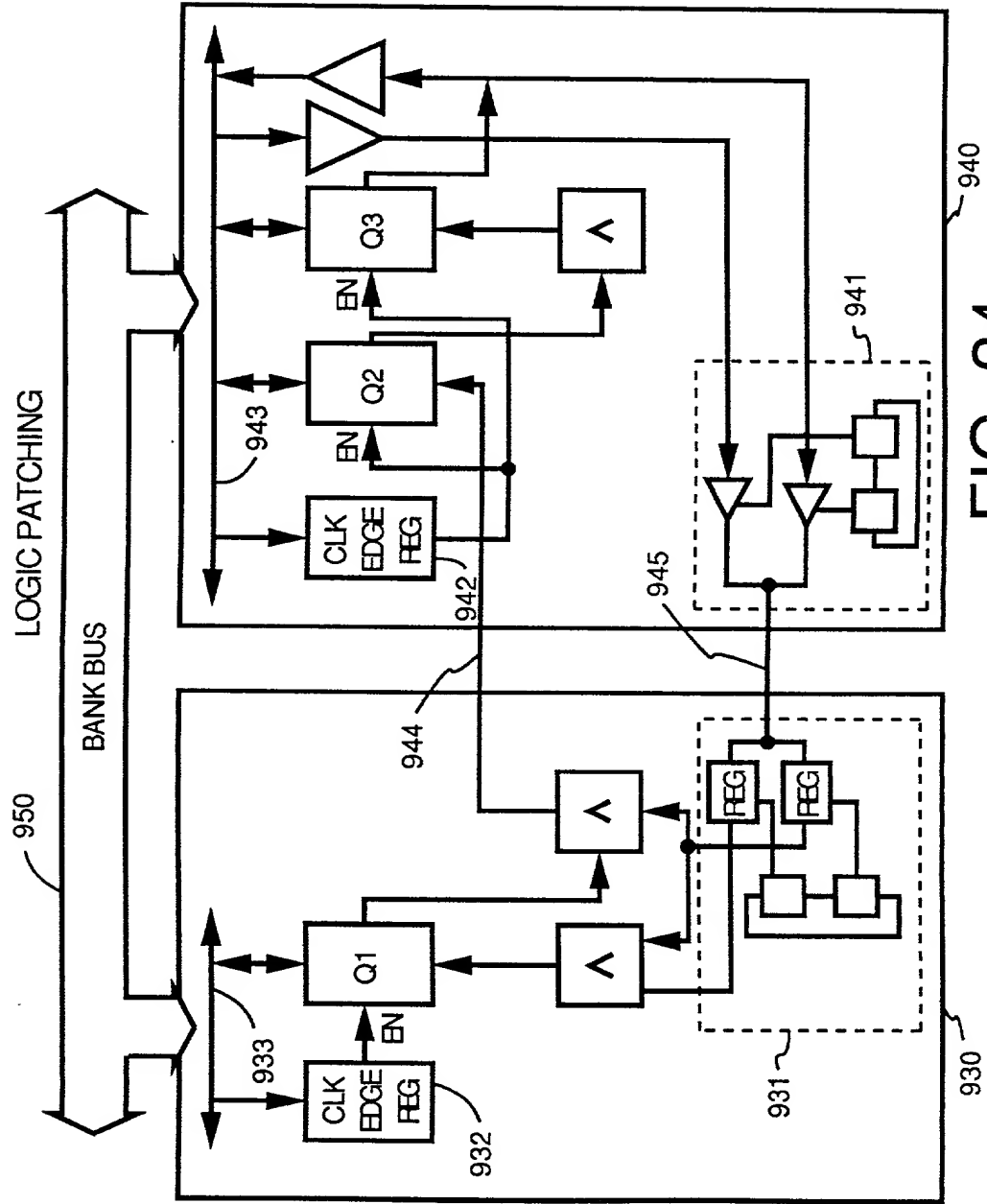


FIG. 34

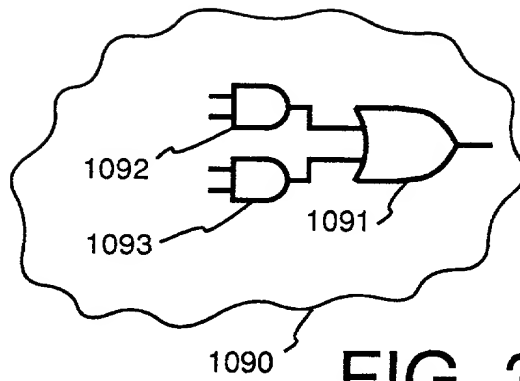


FIG. 35a

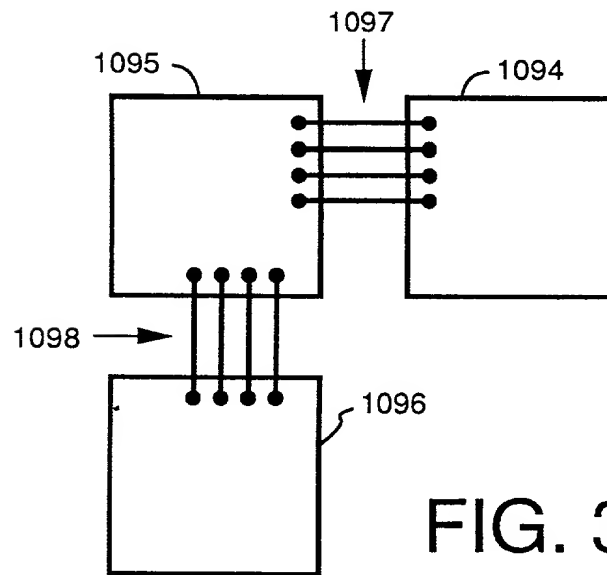


FIG. 35b

FIG. 35c

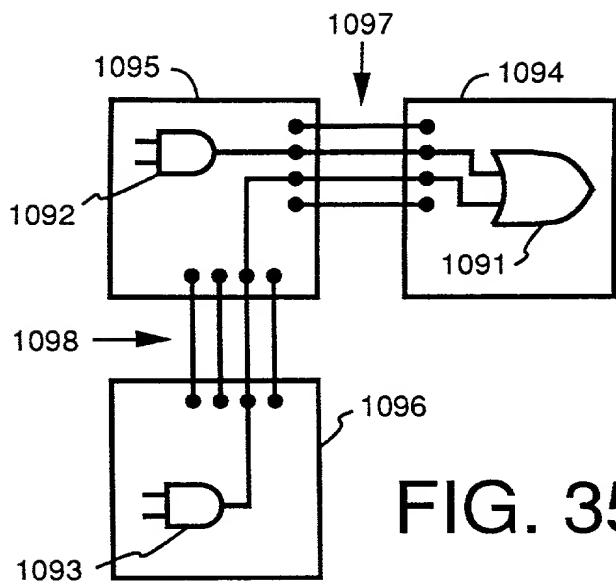


FIG. 35c

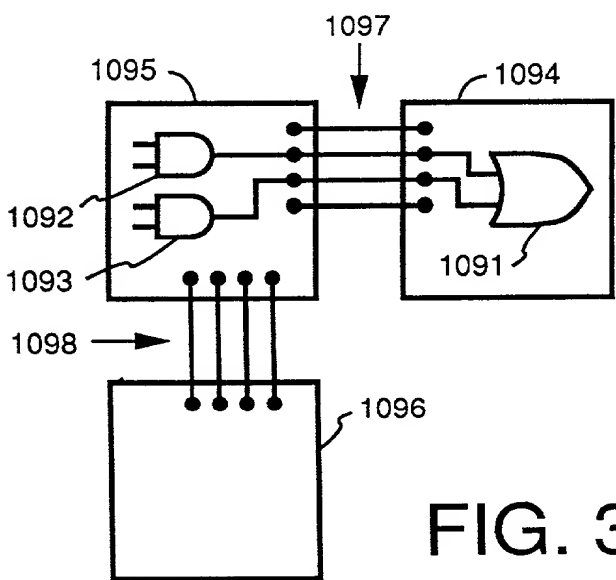


FIG. 35d

I/O PIN OVERVIEW OF
FPGA LOGIC DEVICE

FPGA : 10K130V, 10K250V WITH
599-PIN PGA PACKAGE

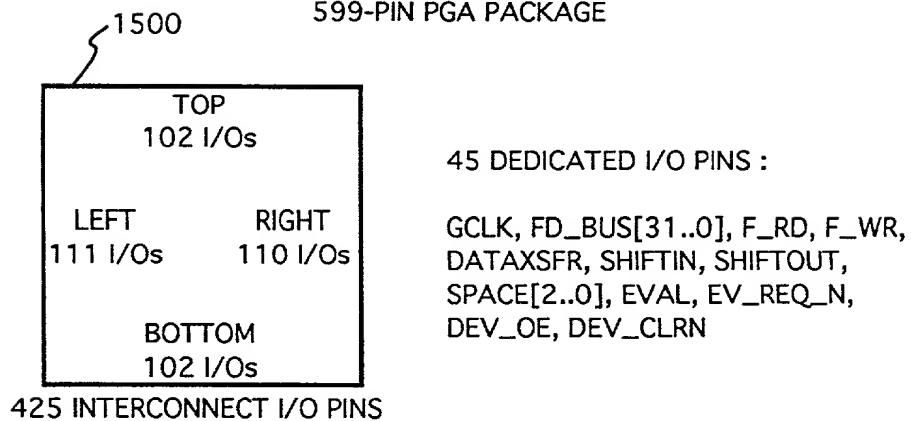


FIG. 36

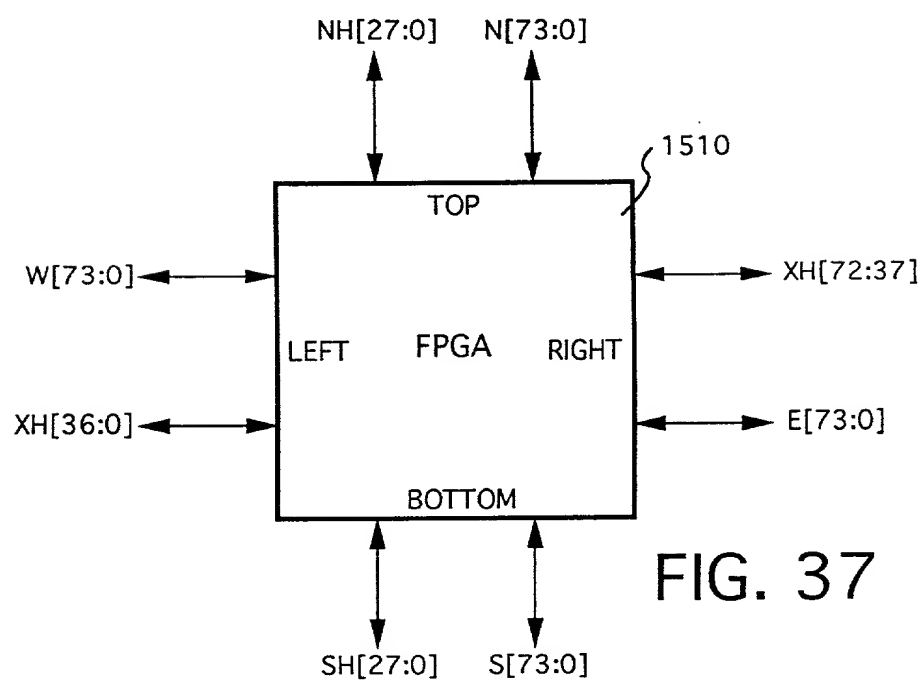


FIG. 37

BOARD CONNECTION - SIDE VIEW

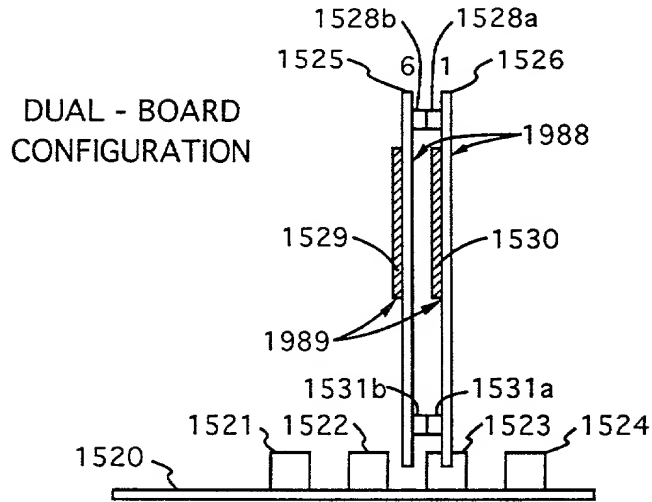


FIG. 38(a)

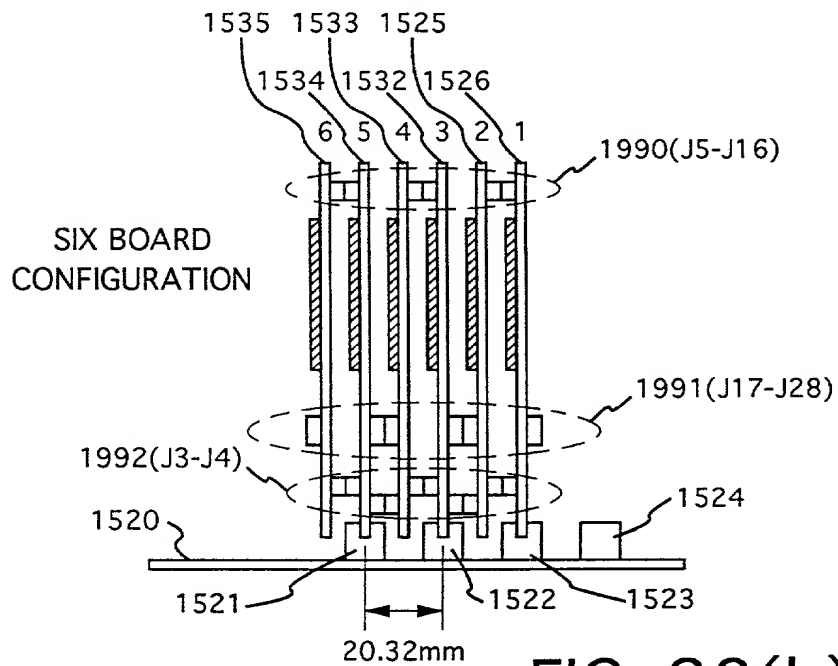


FIG. 38(b)

SIX-BOARD CONFIGURATION DIRECT-NEIGHBOR AND ONE-HOP FPGA ARRAY-X TORUS, Y MESH

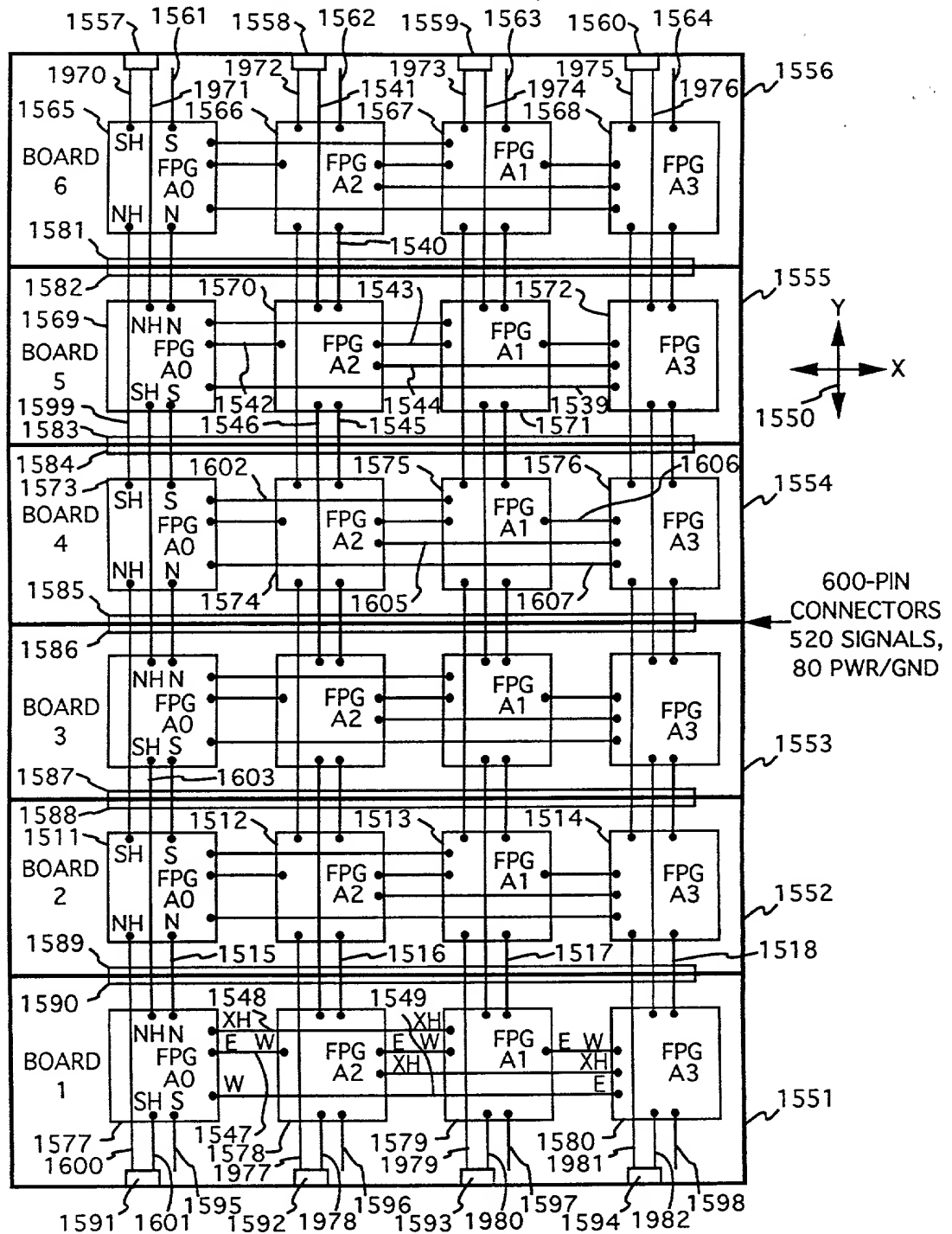


FIG. 39

FPGA ARRAY CONNECTION BETWEEN BOARDS

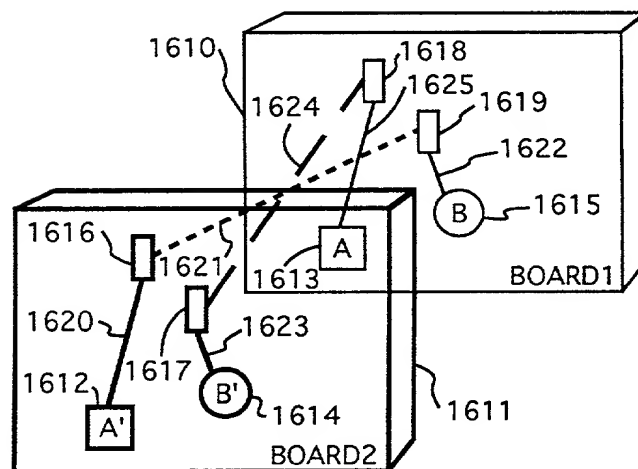


FIG. 40(a)

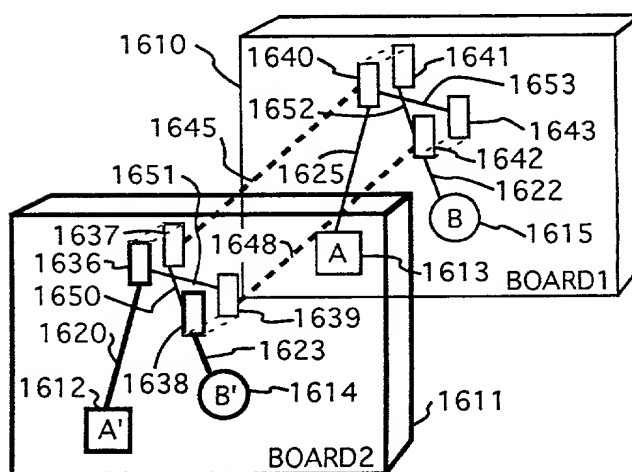
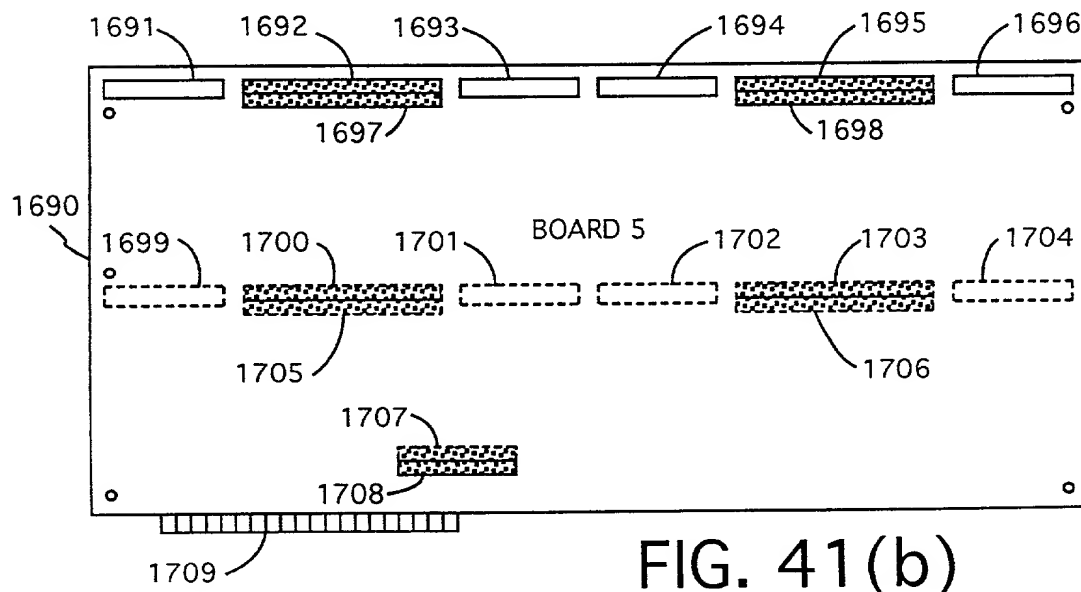
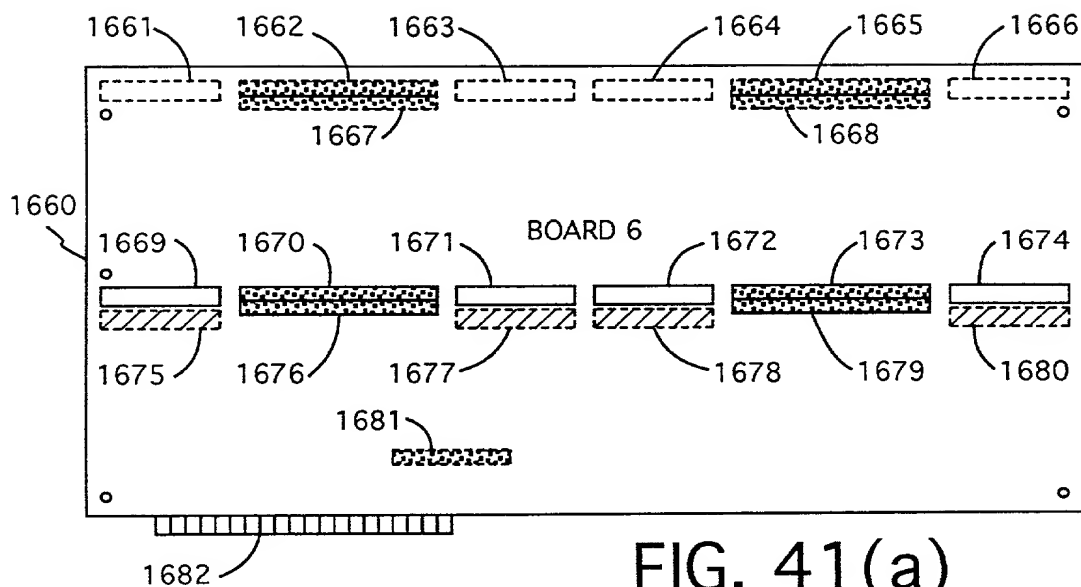
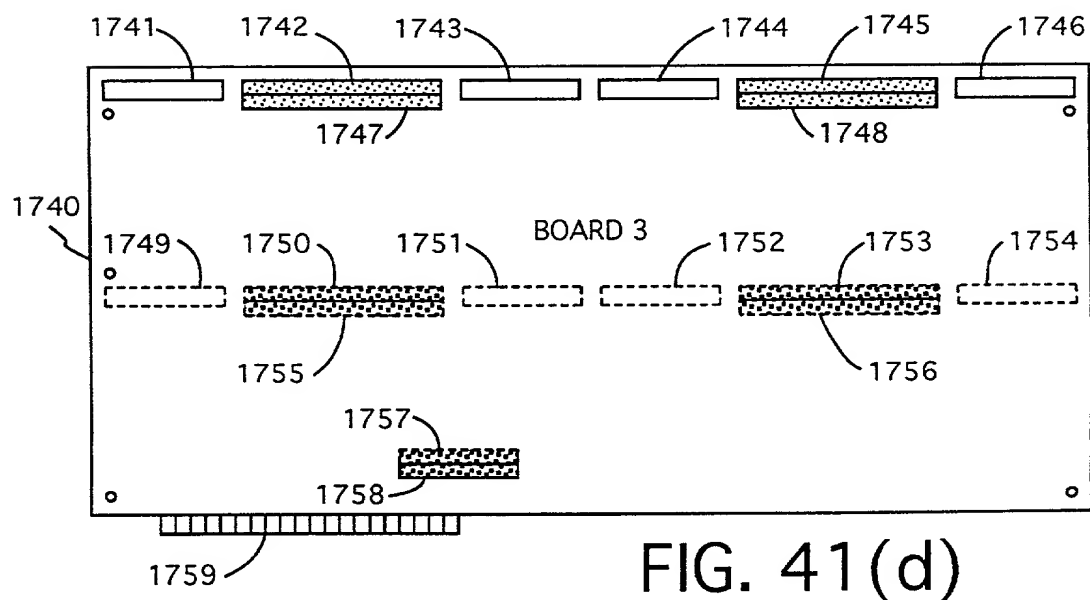
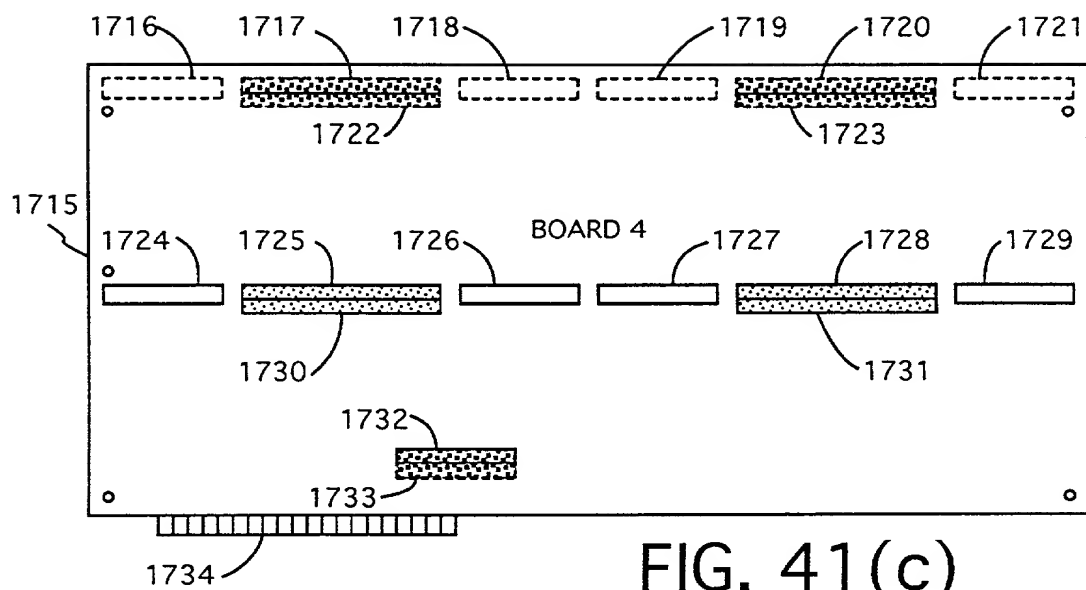


FIG. 40(b)





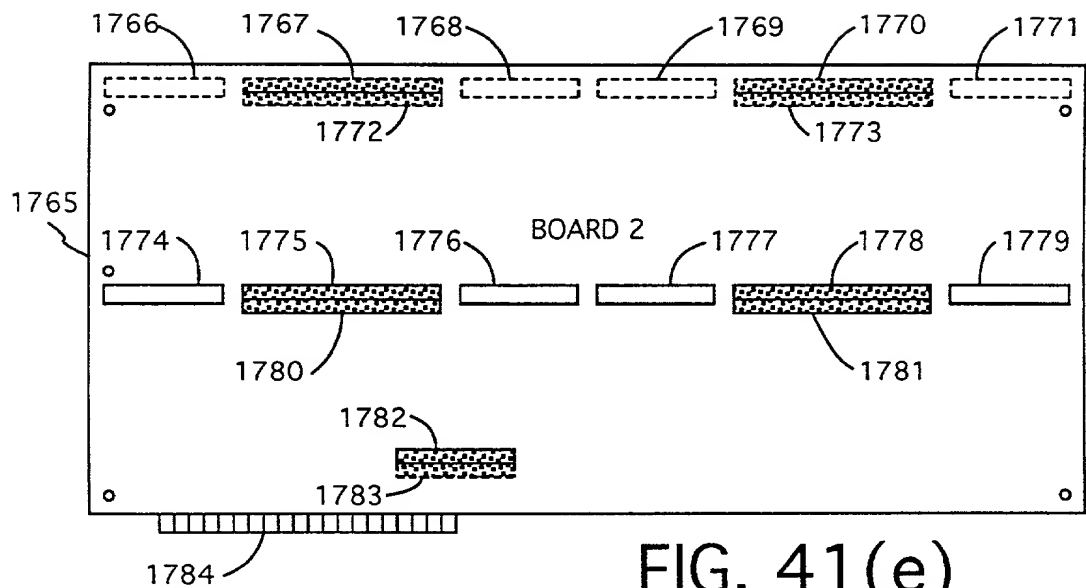


FIG. 41(e)

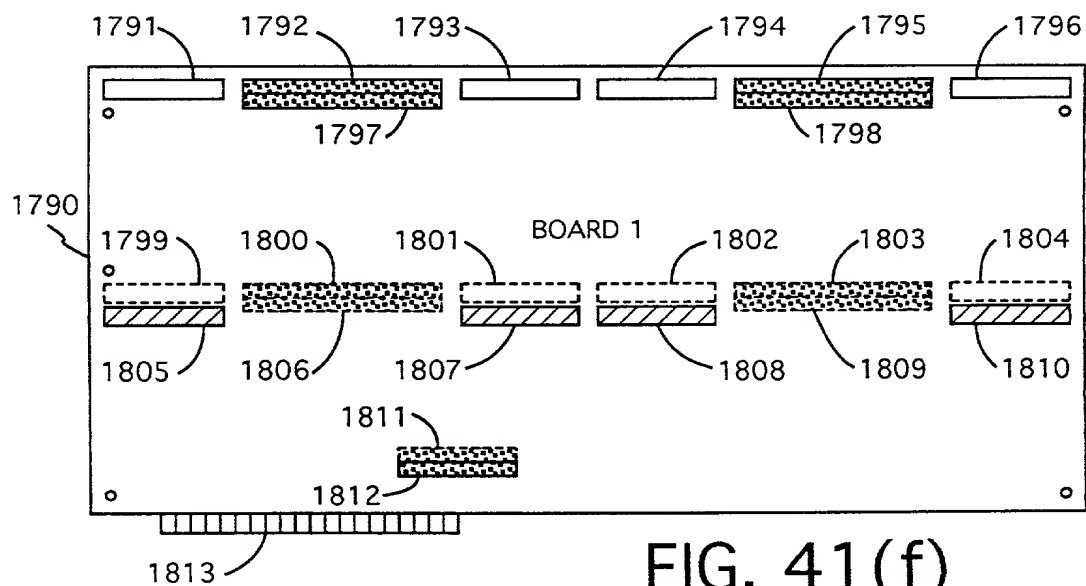


FIG. 41(f)

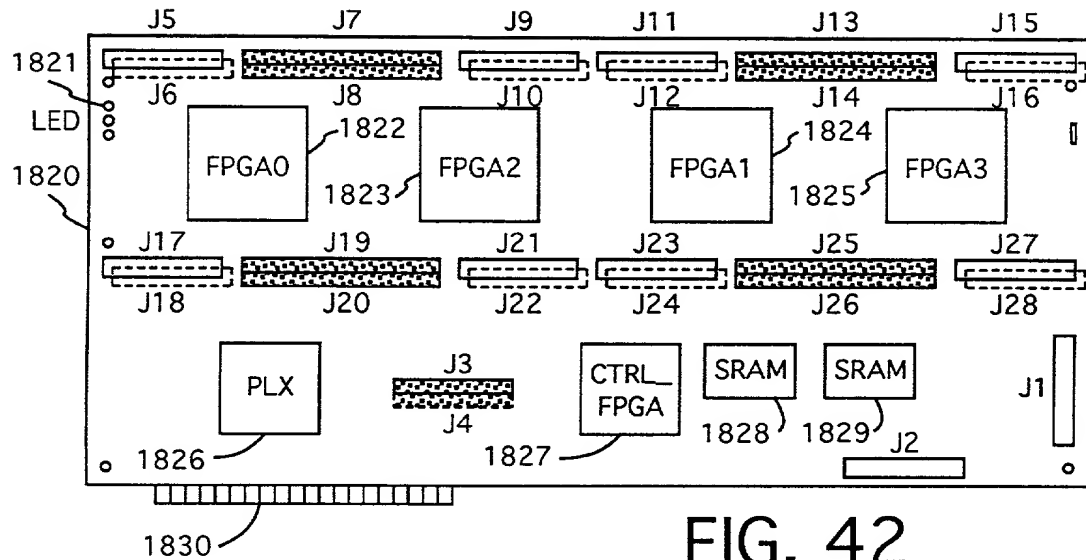


FIG. 42

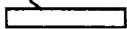
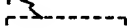


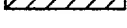

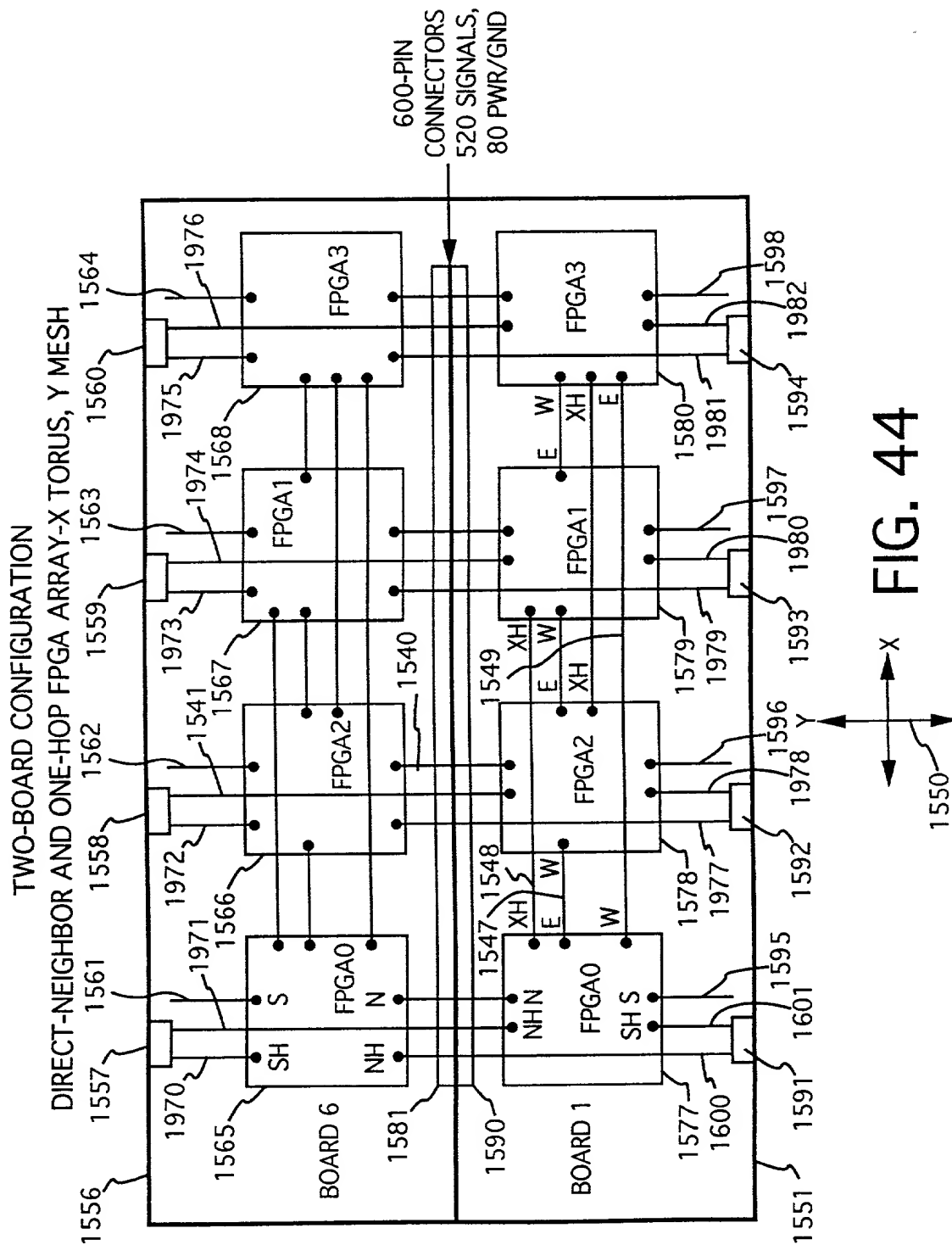
- 1840  2x30 HEADER, SMD, COMPONENT SIDE
- 1841  2x30 RECEPTACLE, SMD, SOLDER SIDE
- 1842  2x45, 2x30 HEADER, THRU HOLE, COMPONENT SIDE
- 1843  2x45, 2x30 RECEPTACLE, THRU HOLE, SOLDER SIDE
- 1844  R-PACK, SMD, COMPONENT SIDE
- 1845  R-PACK, SMD, SOLDER SIDE

FIG. 43



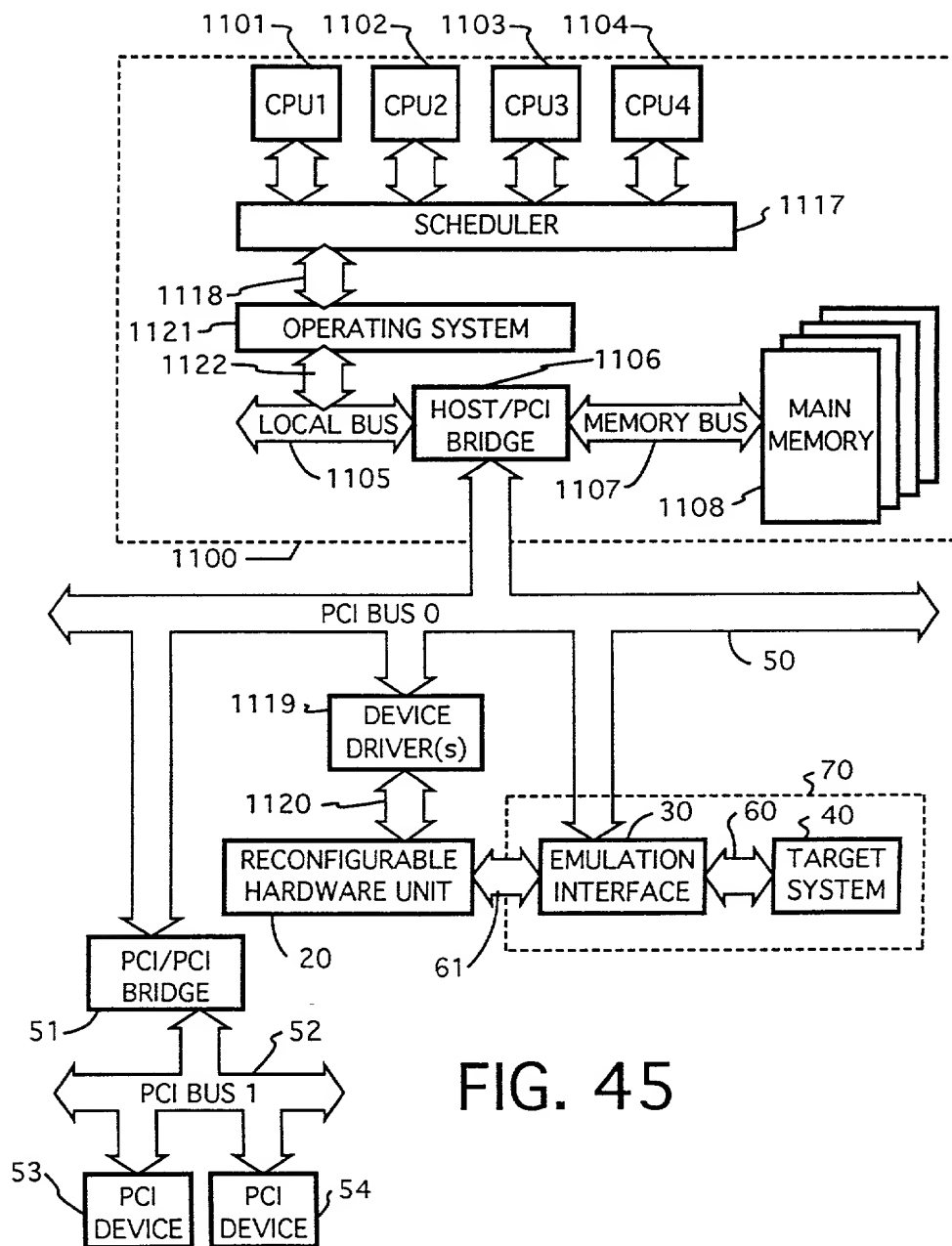


FIG. 45

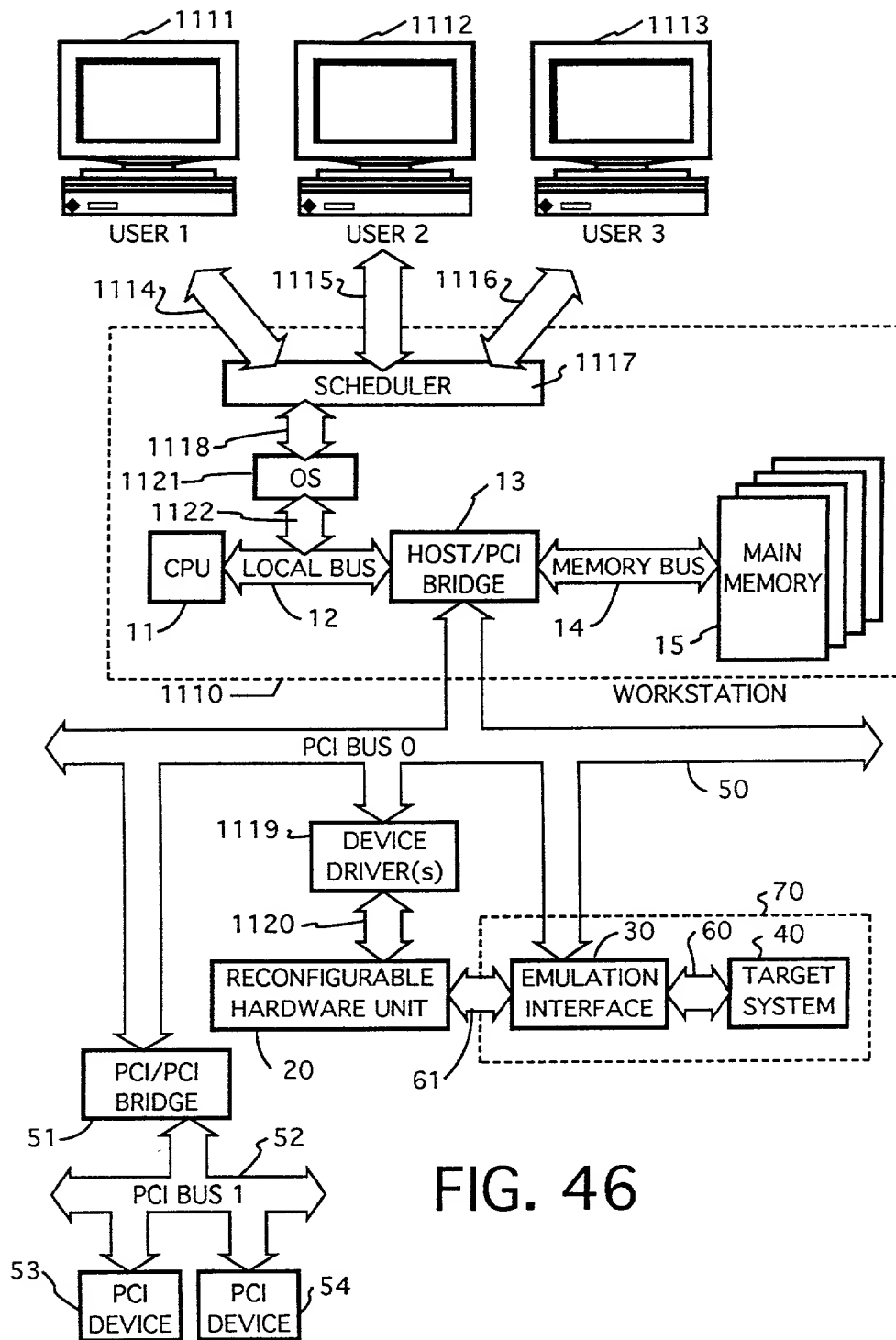


FIG. 46

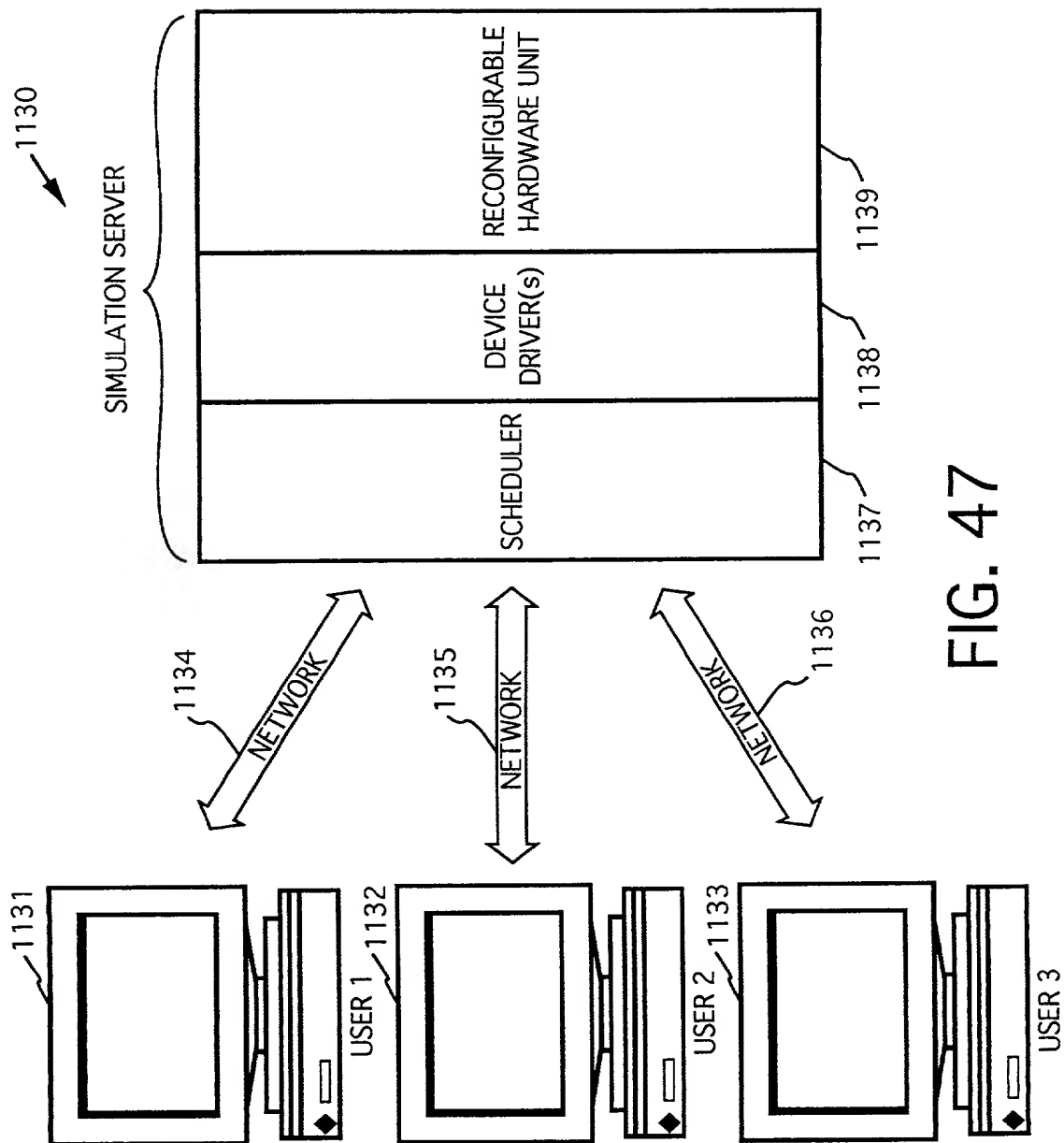


FIG. 47

SIMULATION SERVER ARCHITECTURE

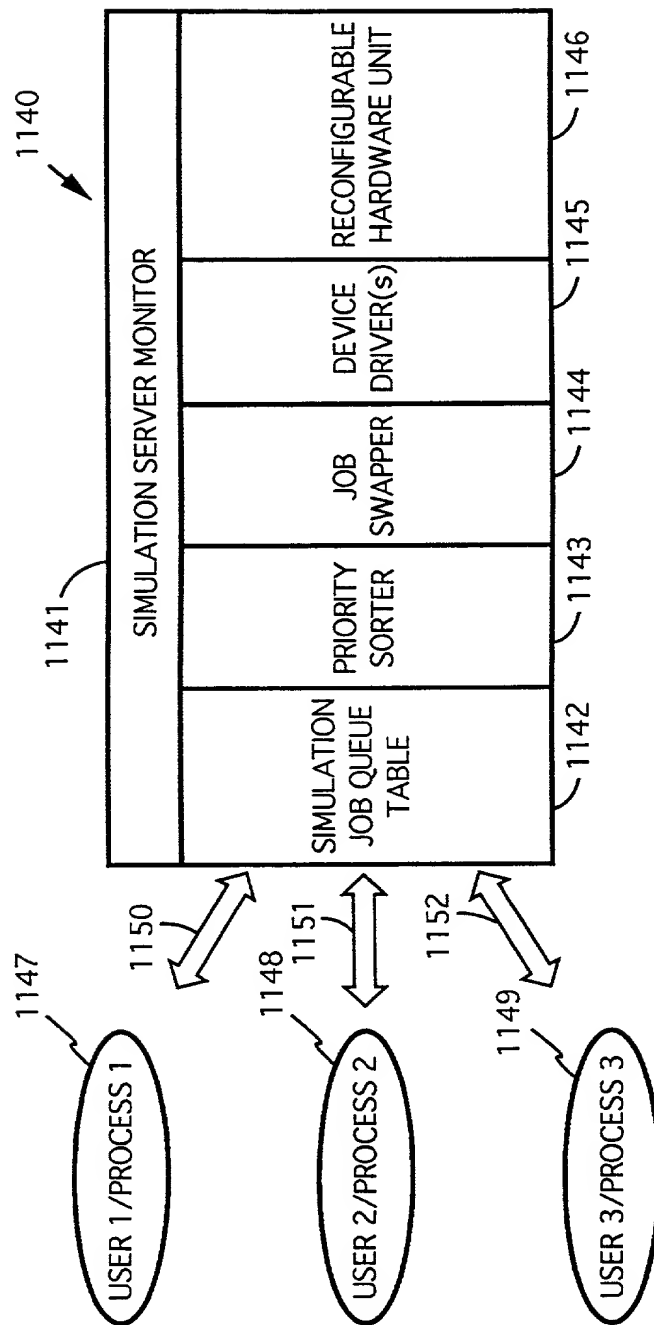


FIG. 48

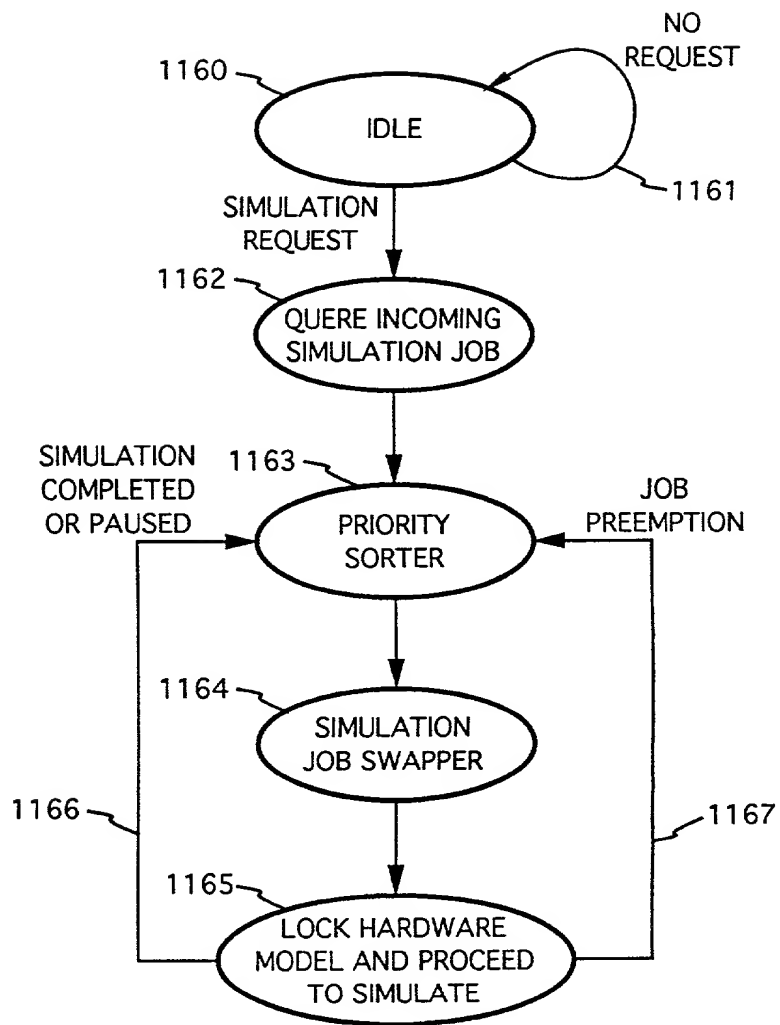


FIG. 49

0950434-1001

JOB SWAPPER

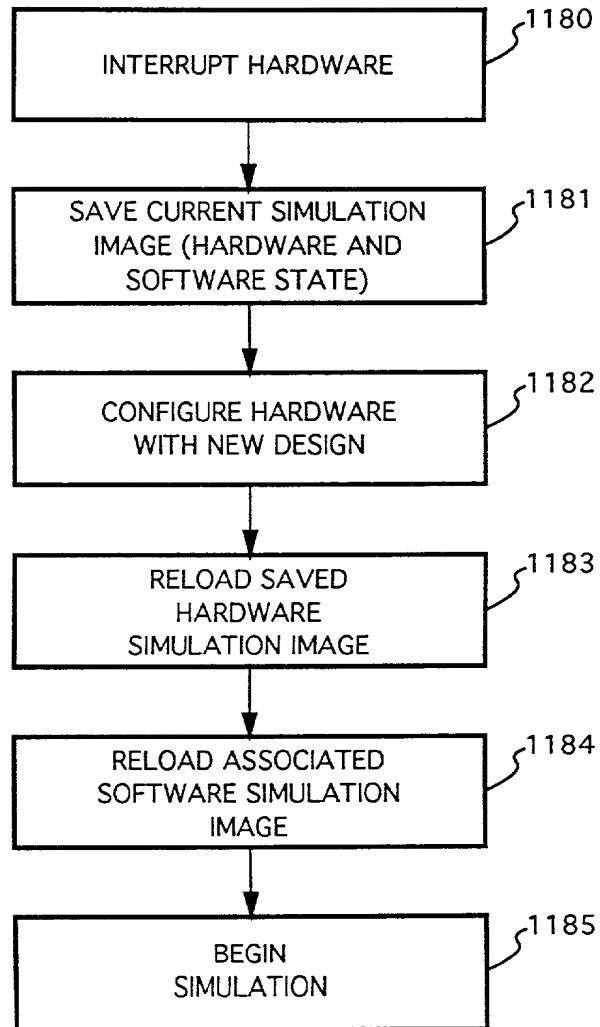


FIG. 50

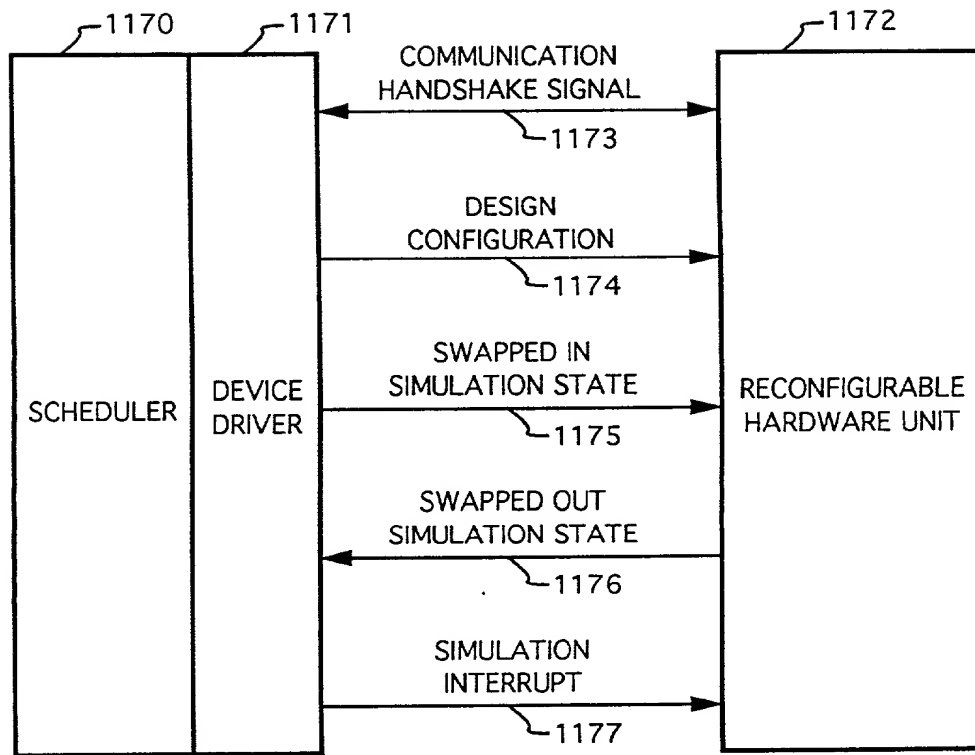


FIG. 51

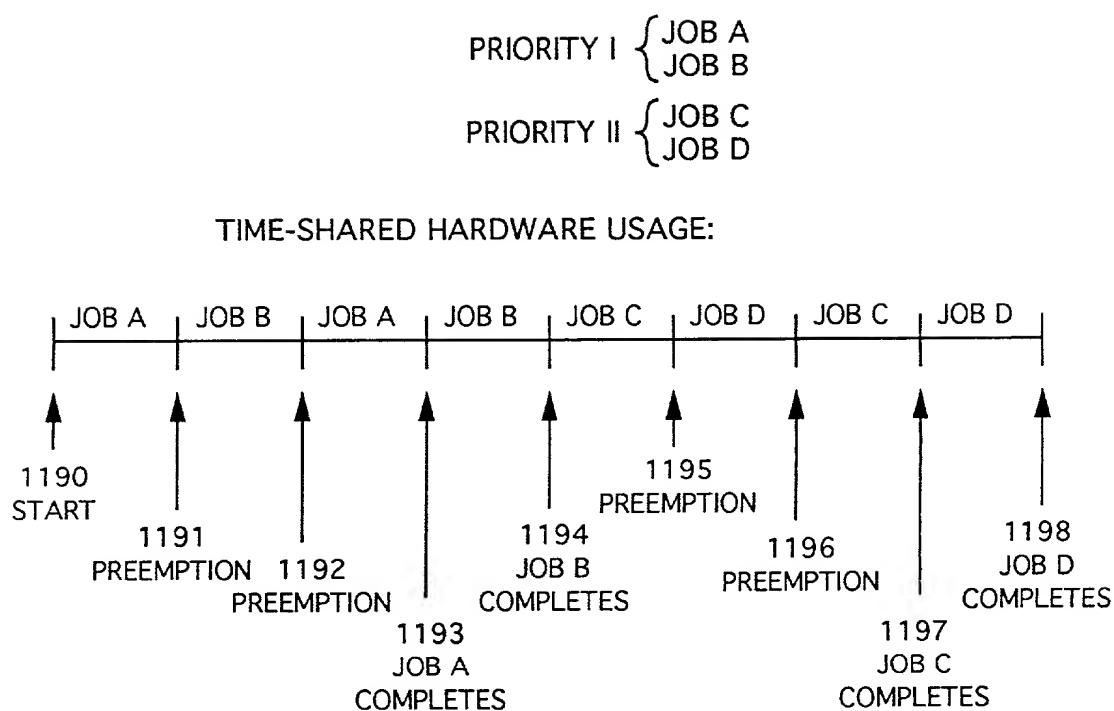


FIG. 52

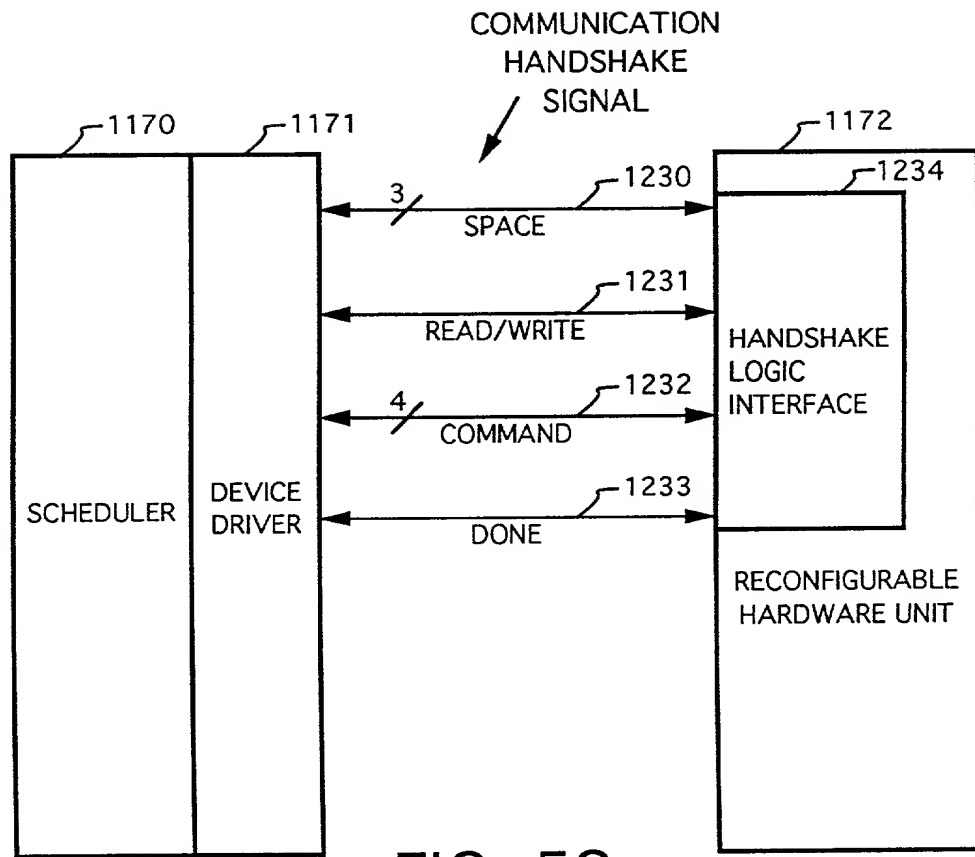


FIG. 53

COMMUNICATION
HANDSHAKE PROTOCOL

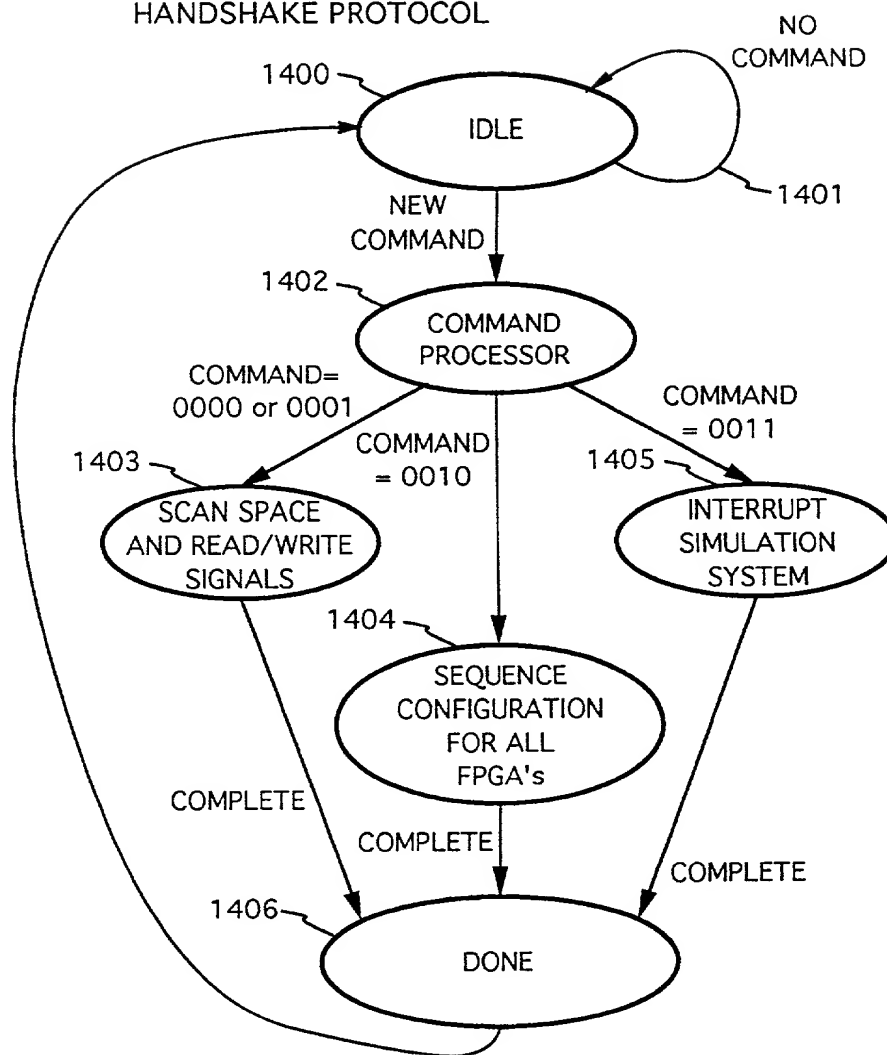


FIG. 54

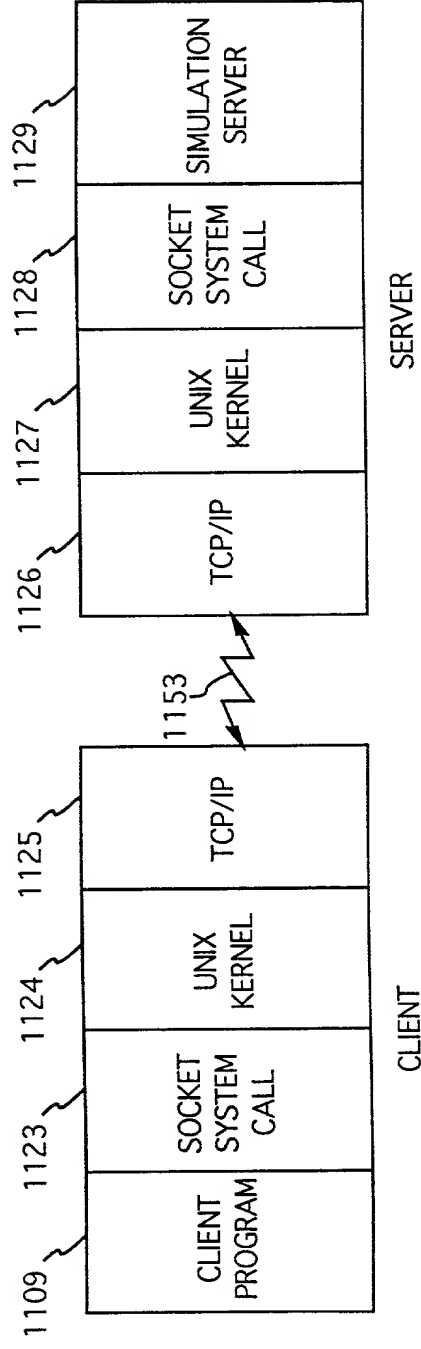
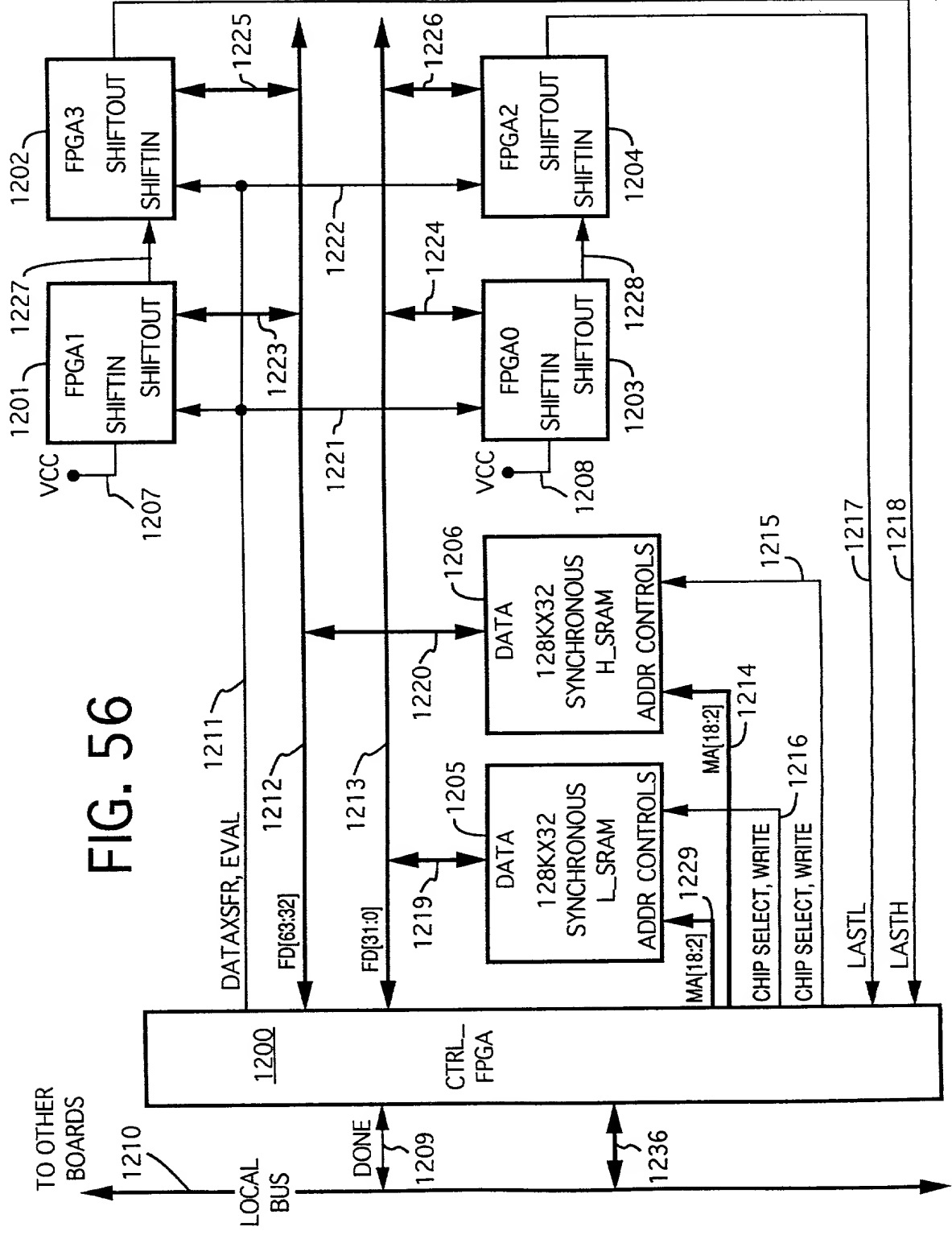


FIG. 55



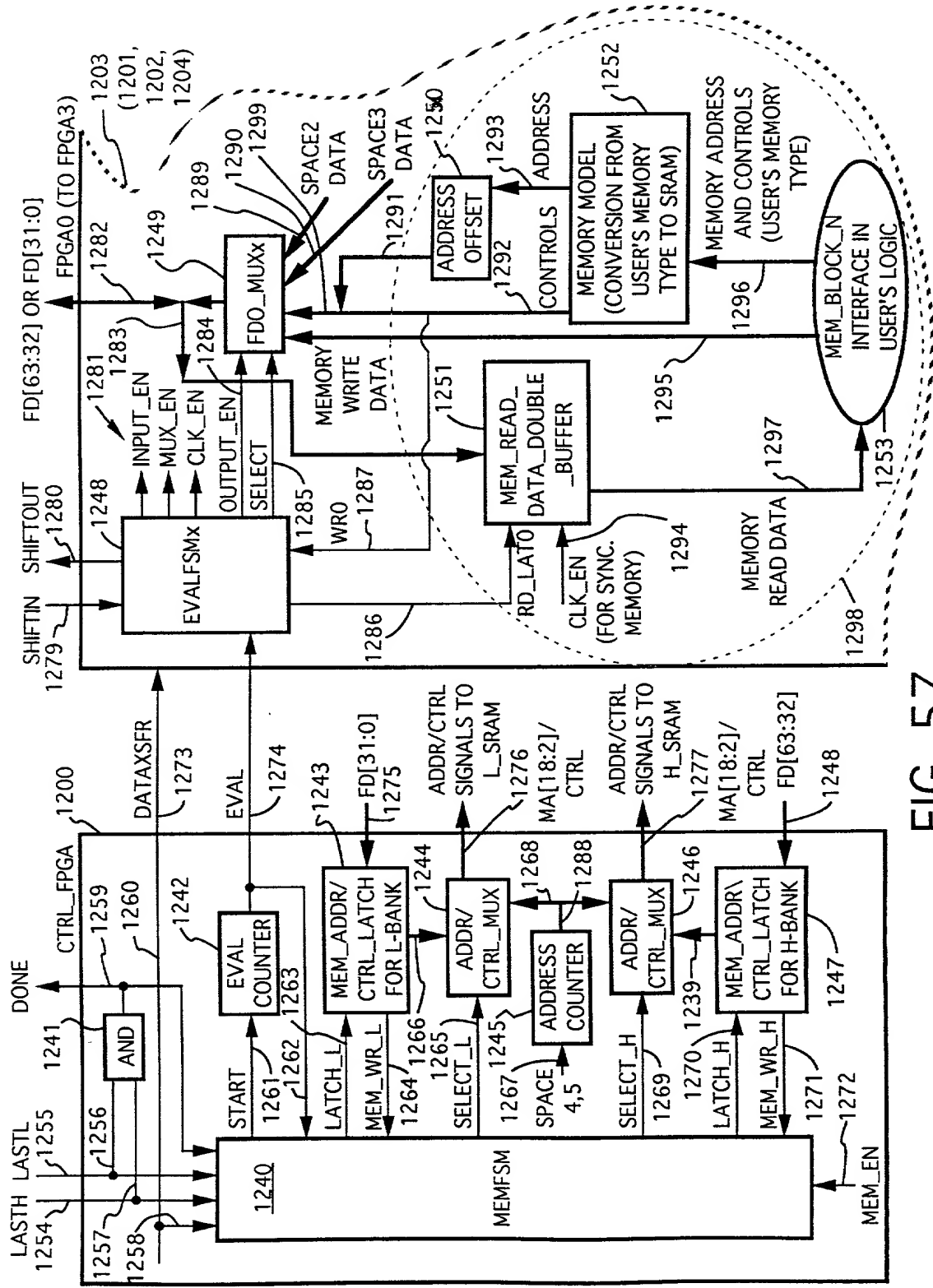
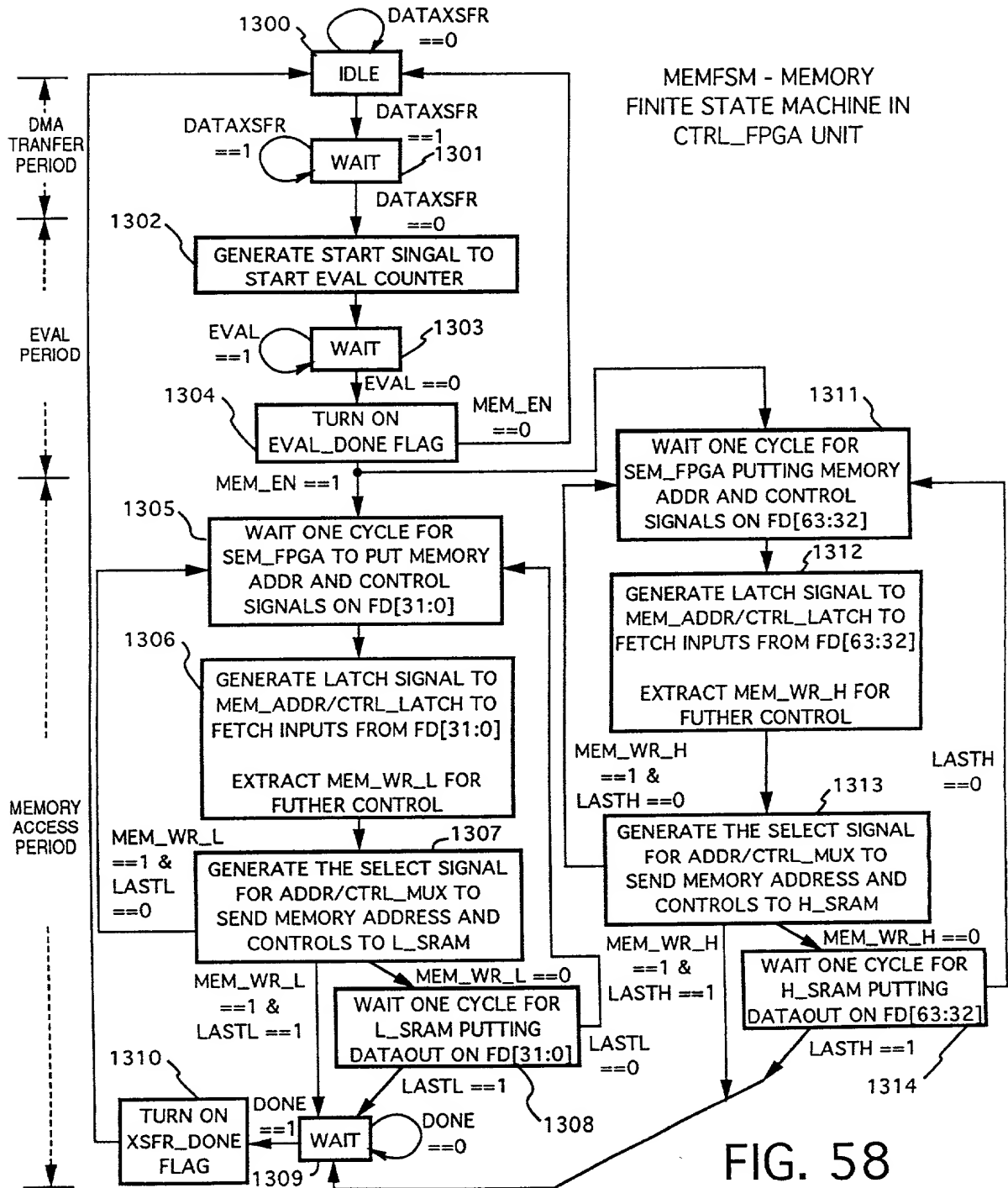


FIG. 57



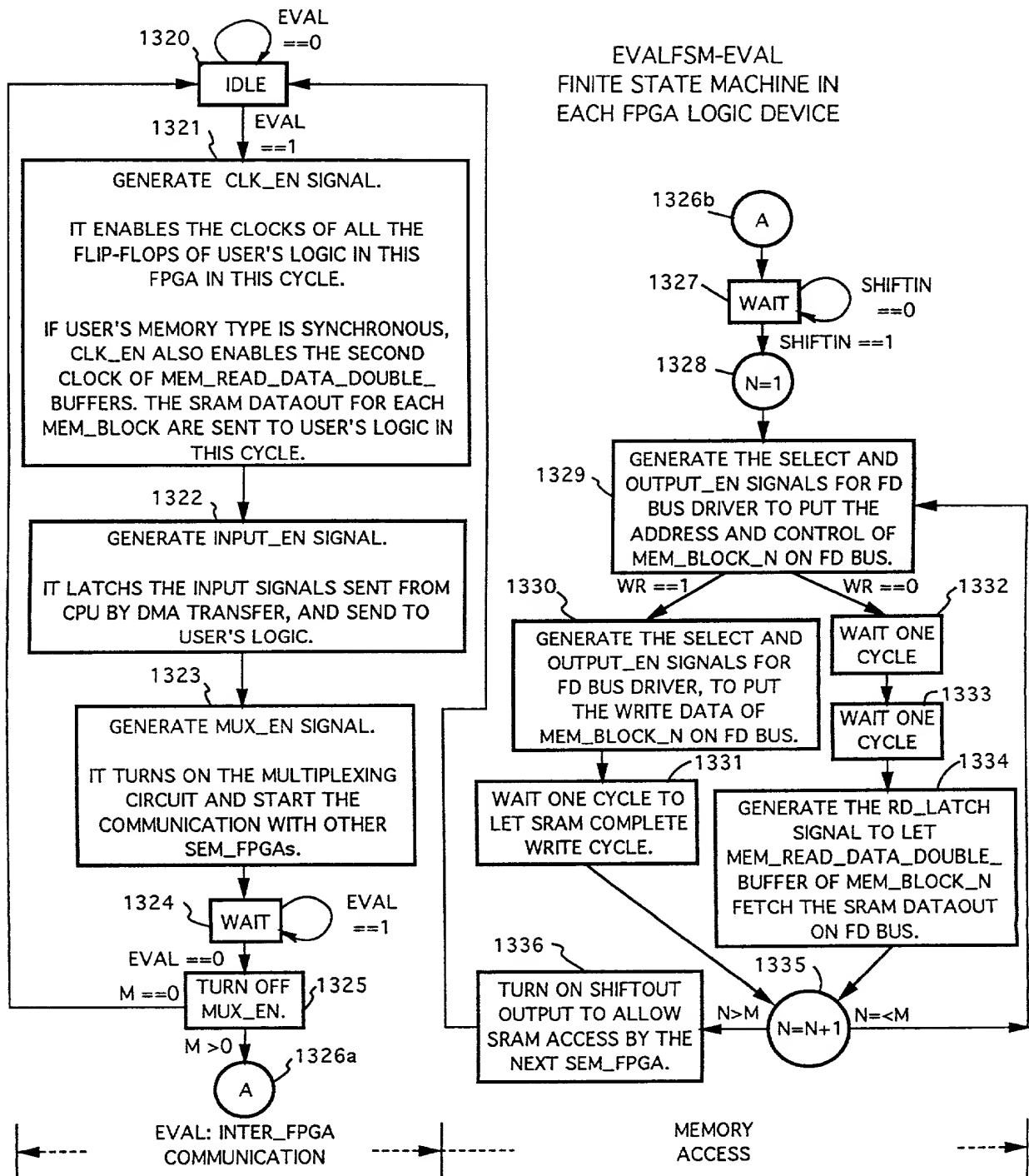
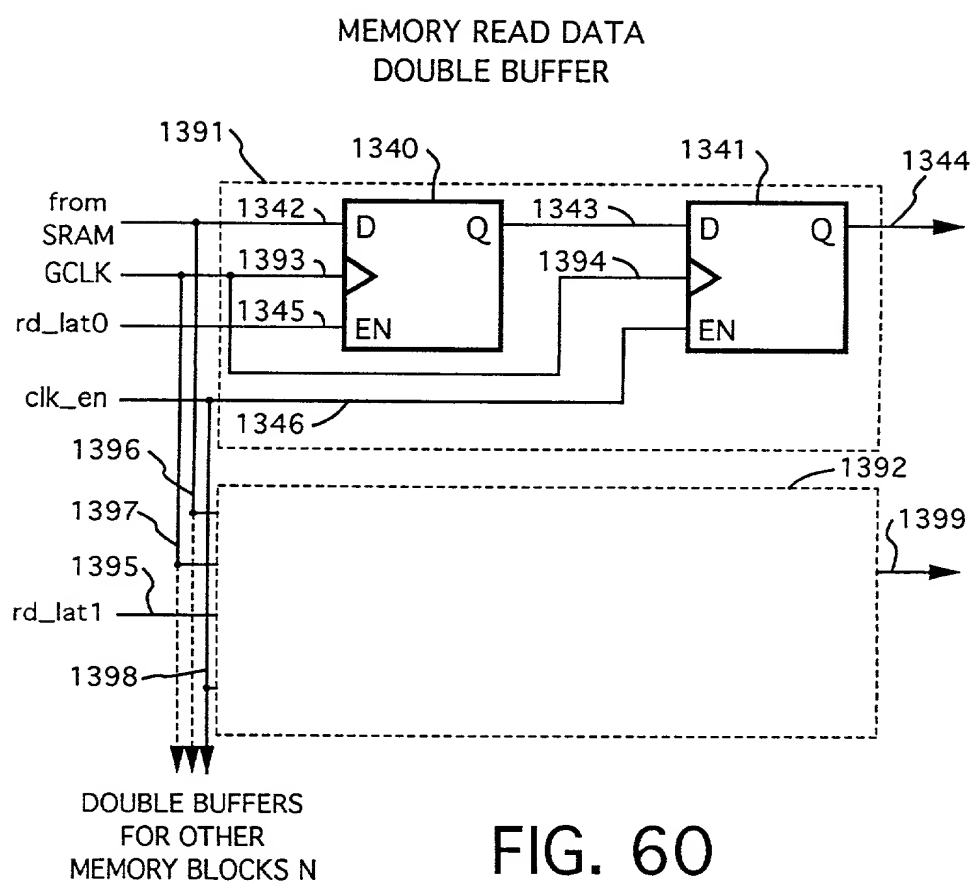
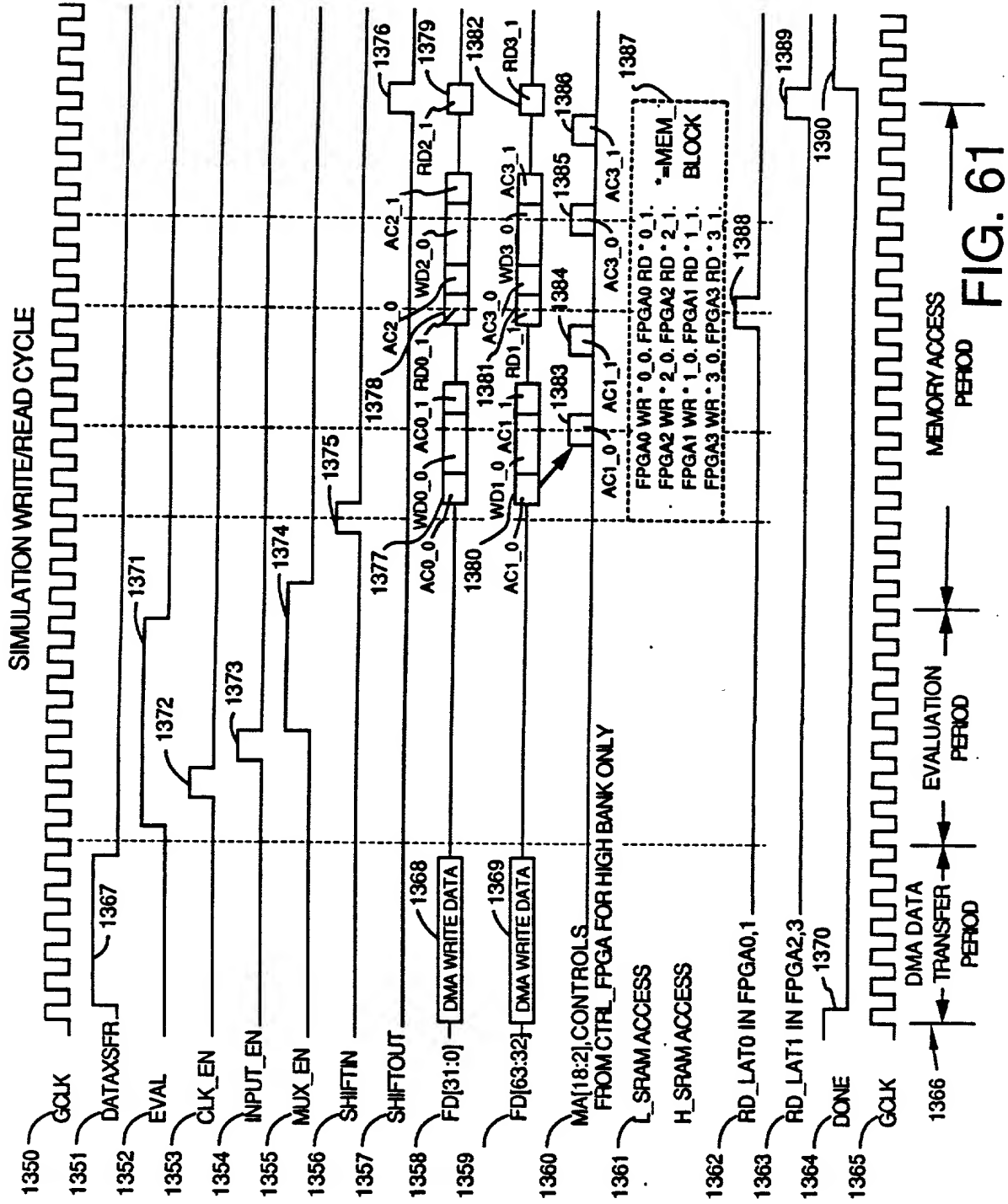
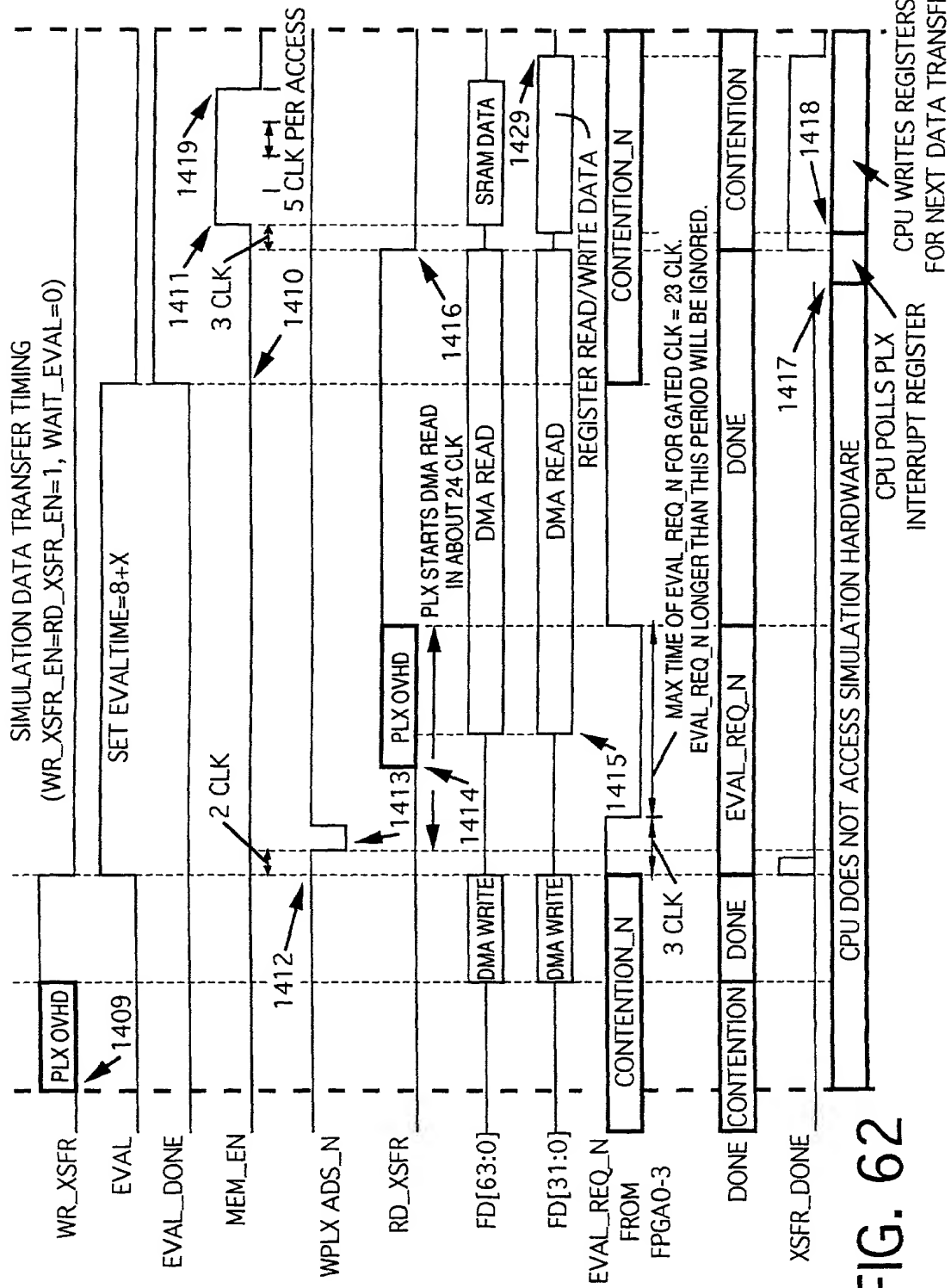
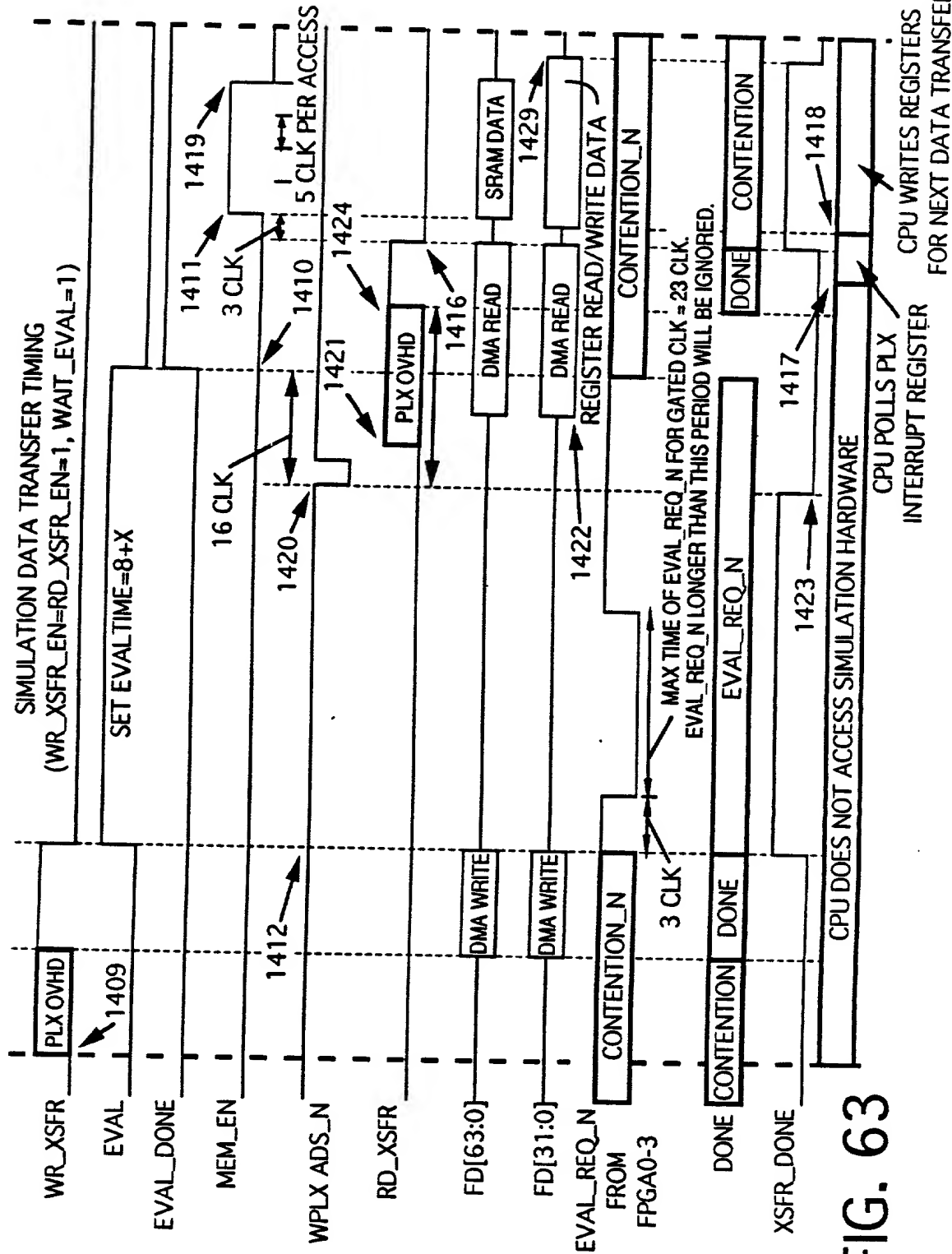


FIG. 59









Typical User Design of PCI Add-on Cards

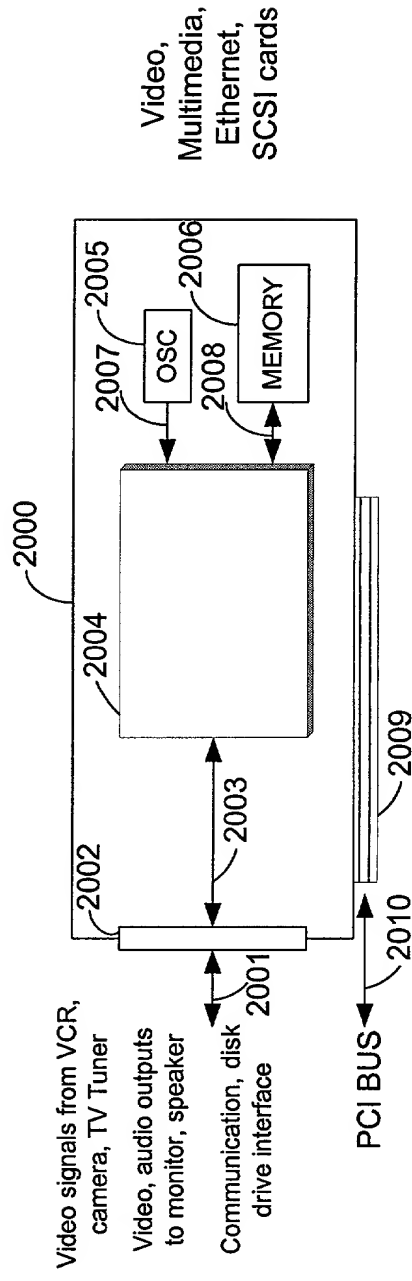
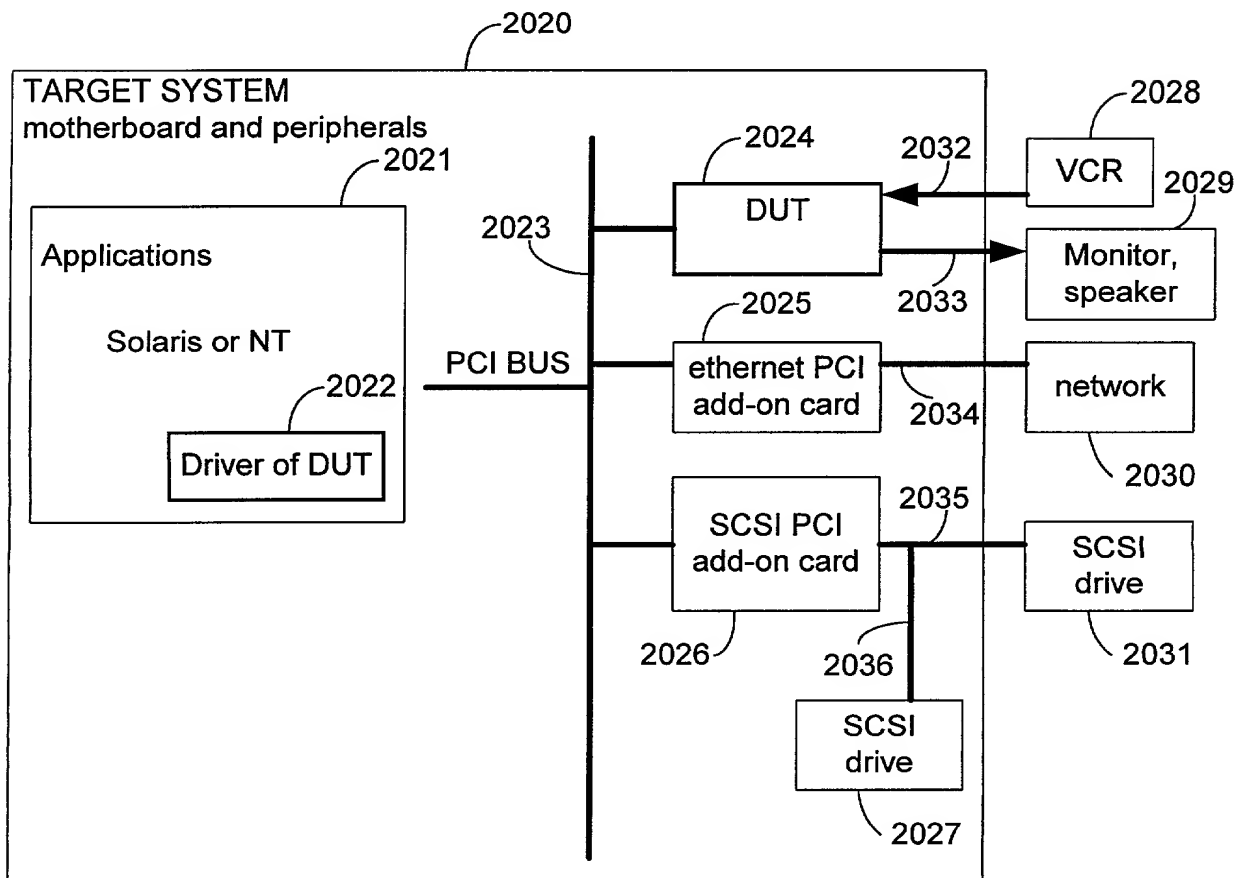


FIG. 64

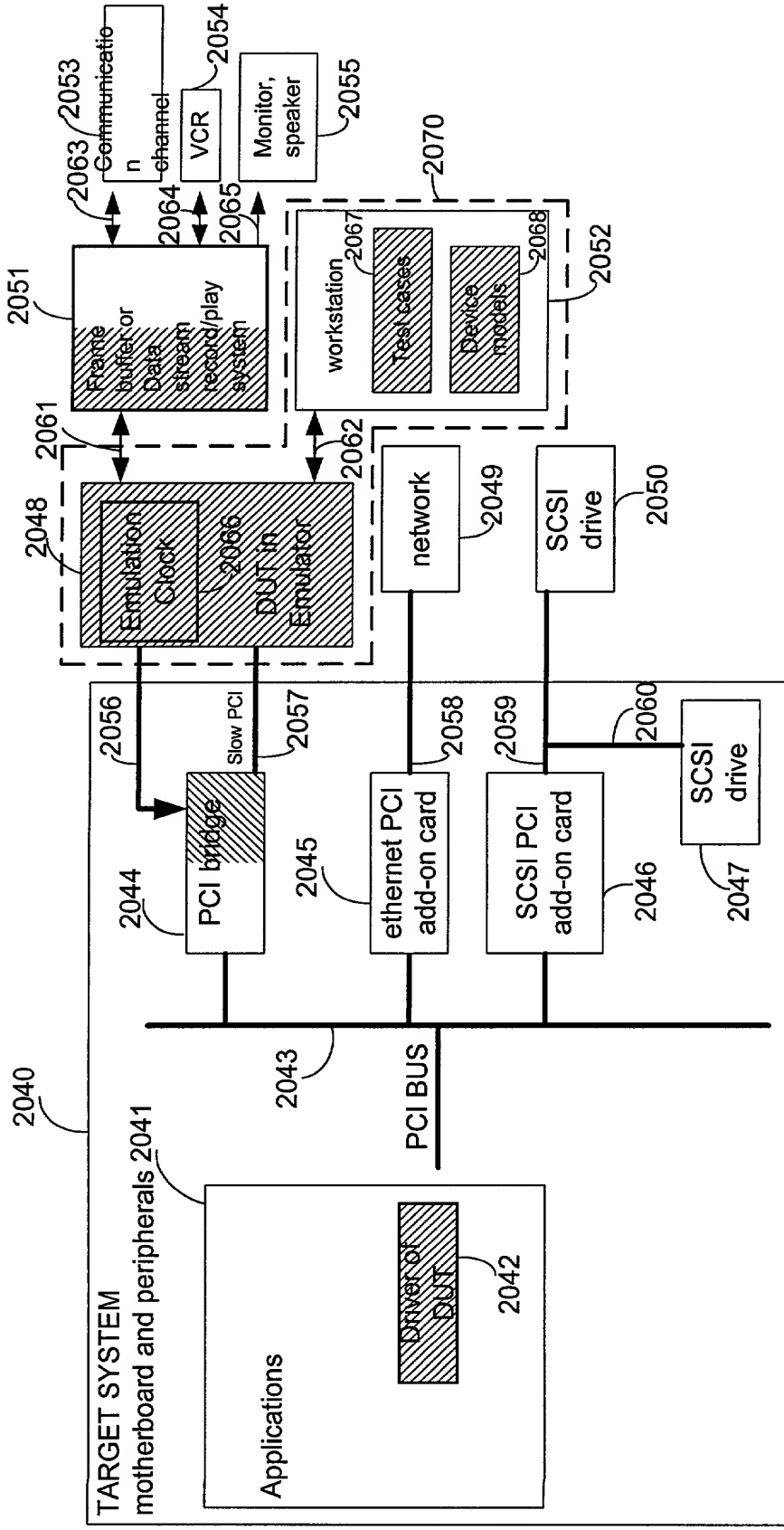
Typical Hardware/Software Co-Verification



 : DUT (Device Under Test)

FIG. 65

Typical Co-Verification by Using Emulator



 : running time at emulation speed

The rest of the target system is running at full speed.

FIG. 66

SIMULATION

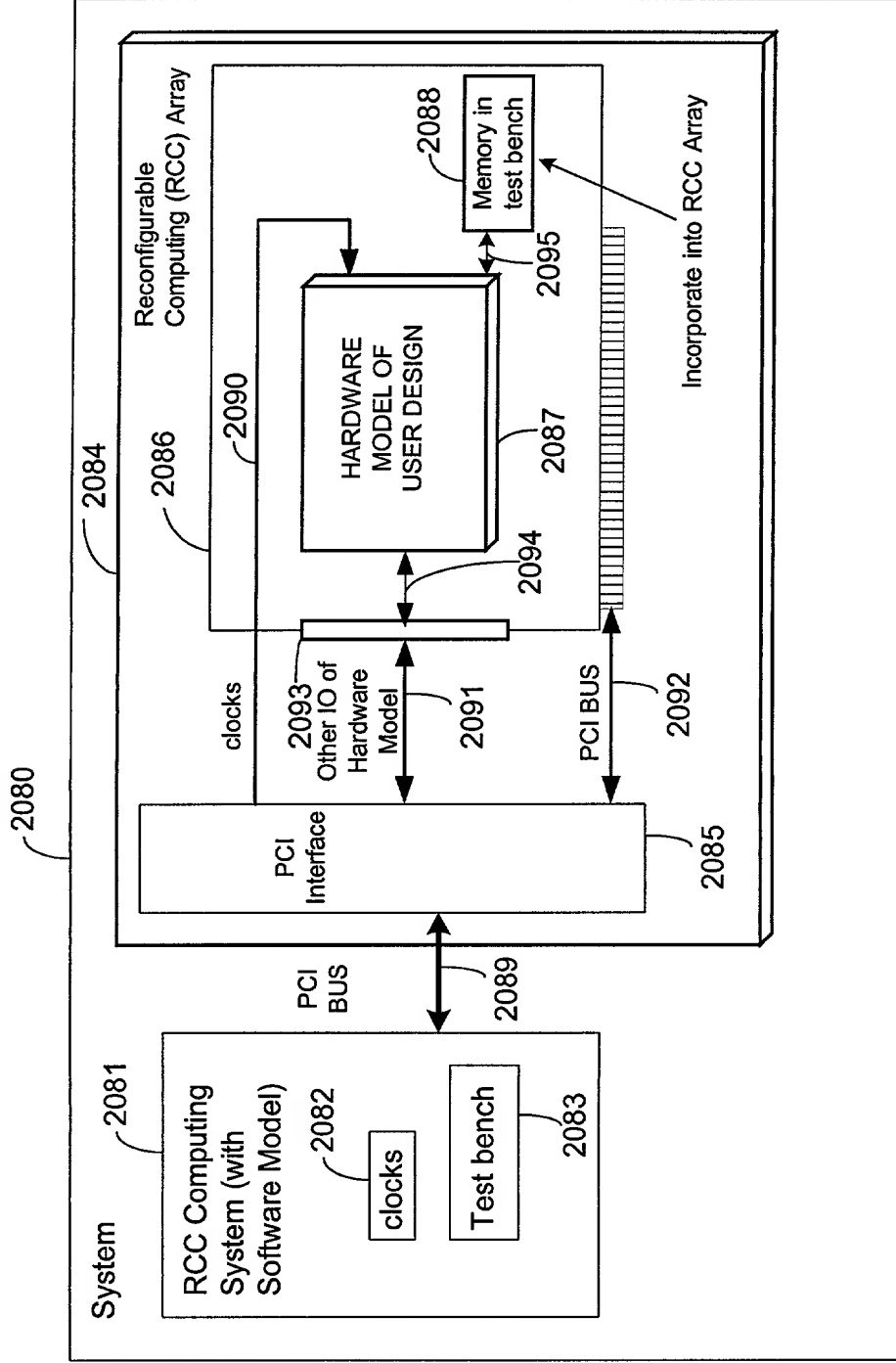


FIG. 67

CO-VERIFICATION WITHOUT EXTERNAL I/O

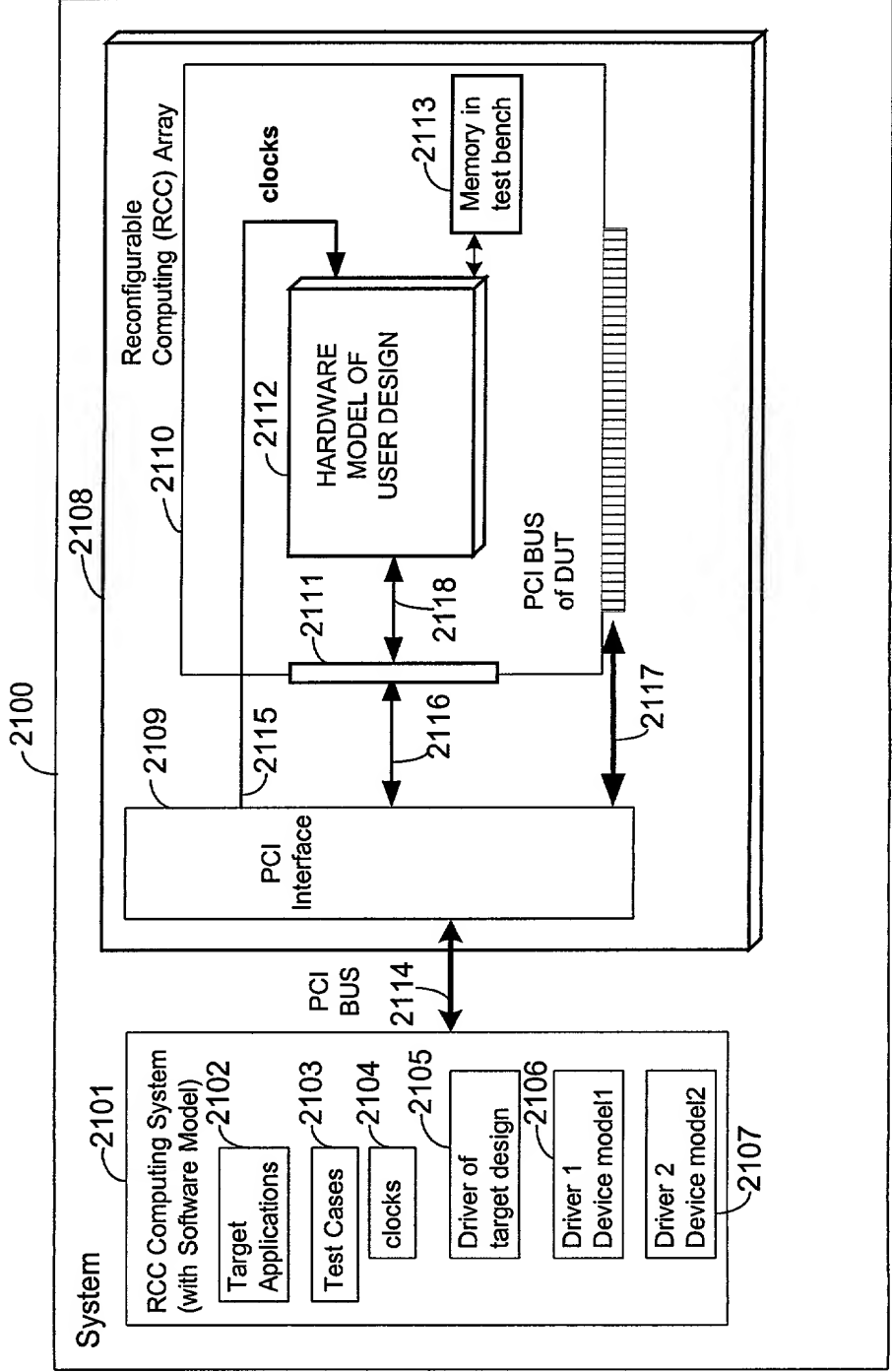


FIG. 68

CO-VERIFICATION WITH EXTERNAL I/O

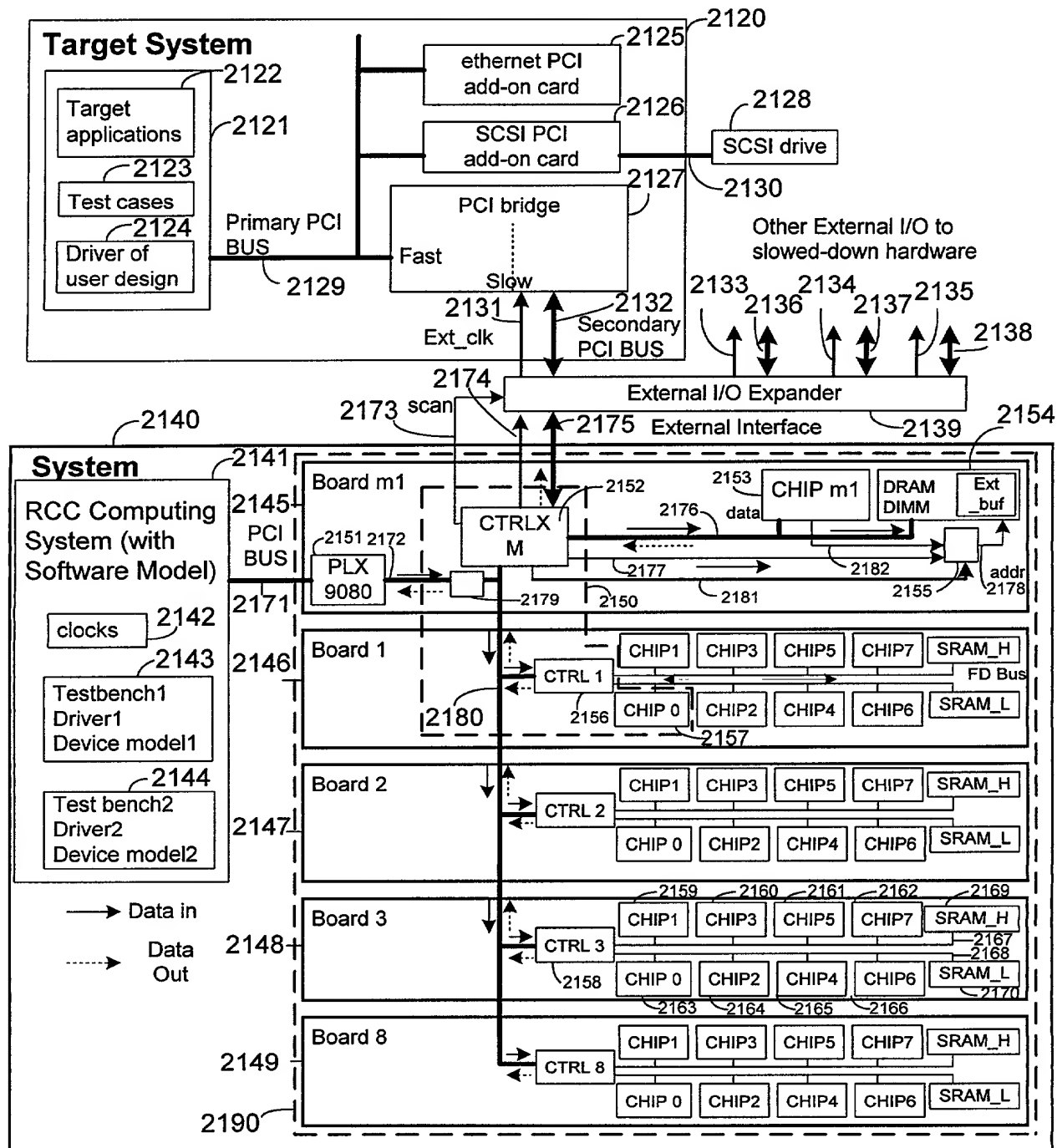


FIG. 69

CONTROL OF DATA-IN CYCLE

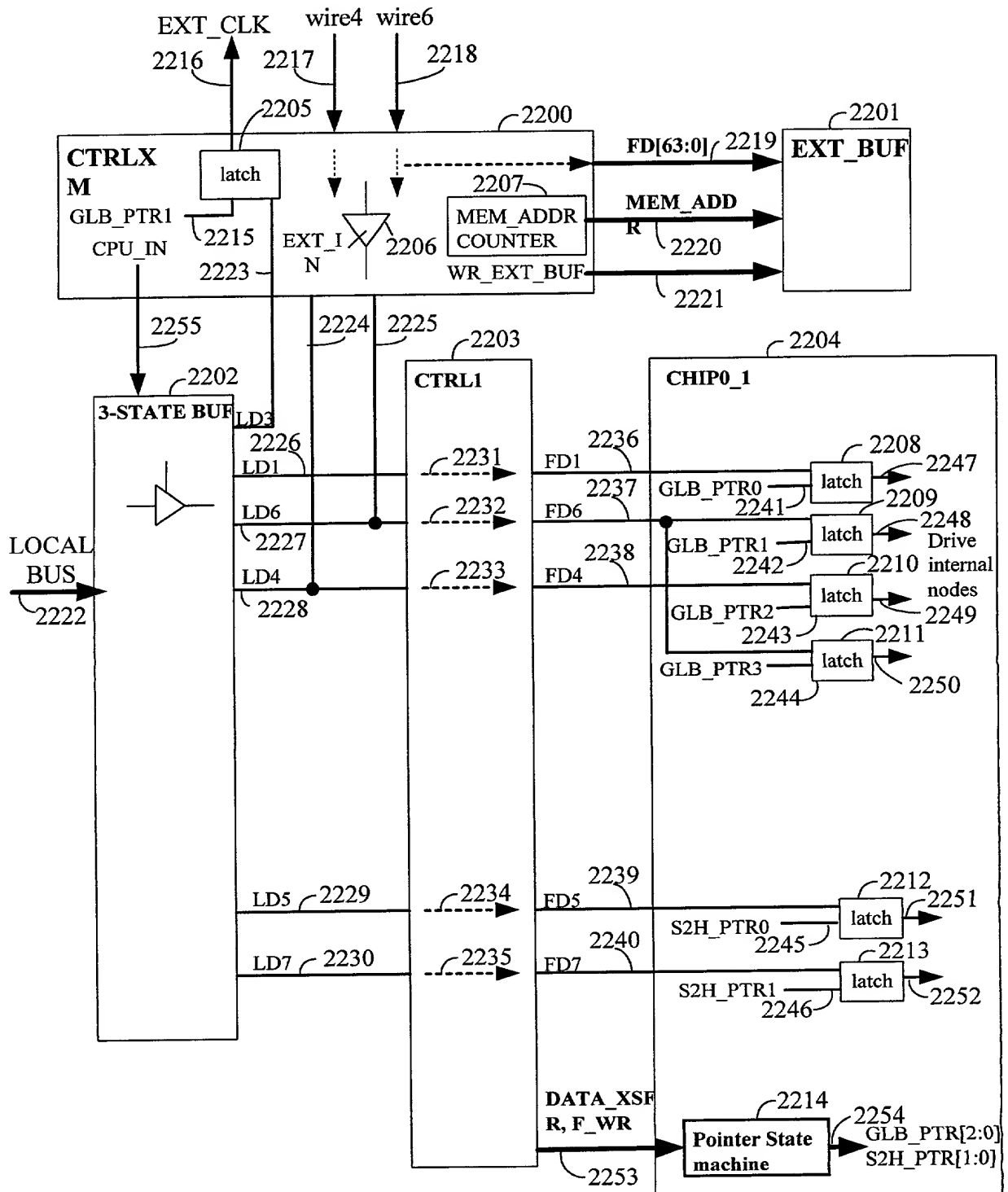


FIG. 70

CONTROL OF DATA-OUT CYCLE

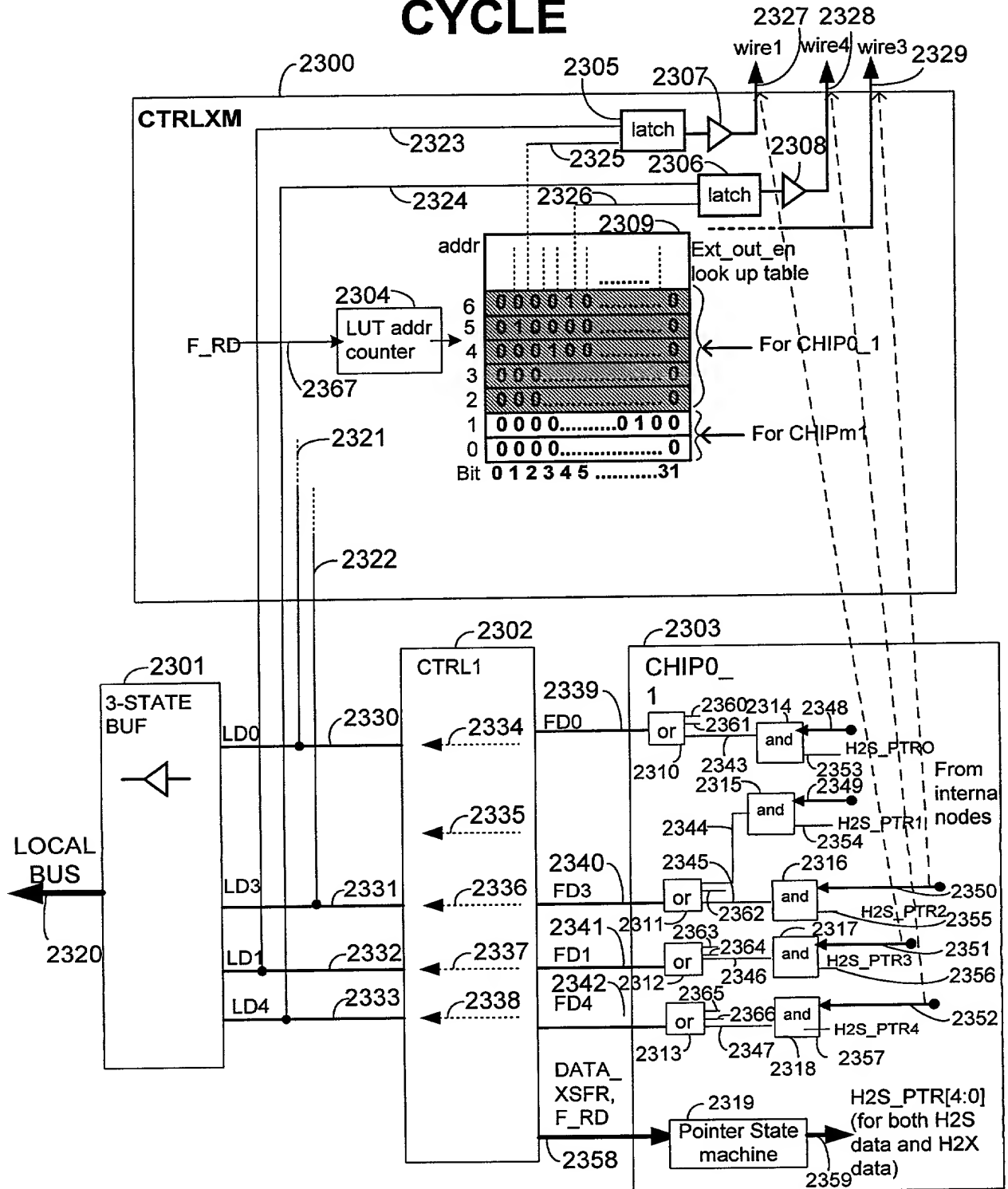


FIG. 71

CONTROL OF DATA-IN CYCLE

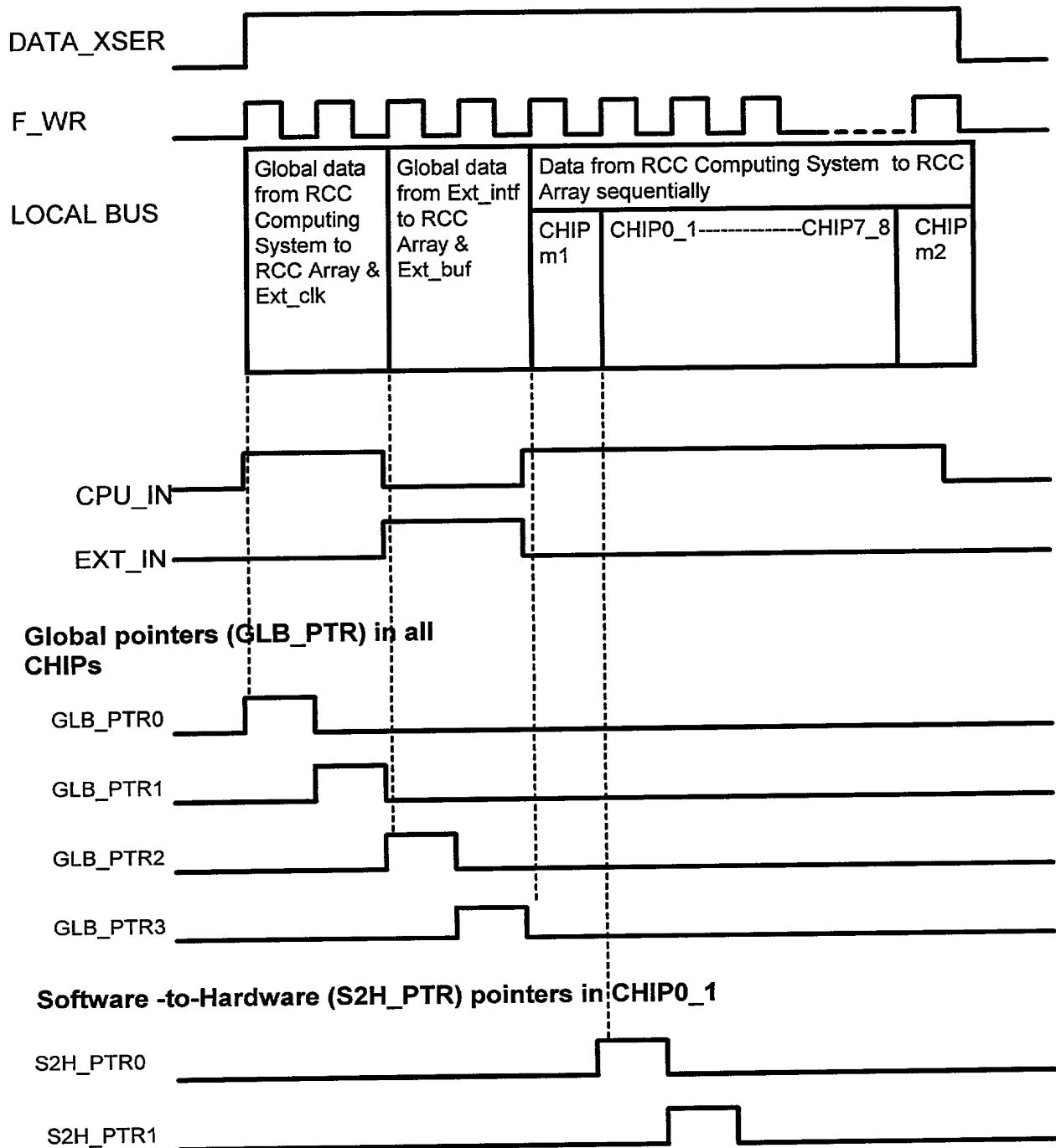


FIG. 72

CONTROL OF DATA-OUT CYCLE

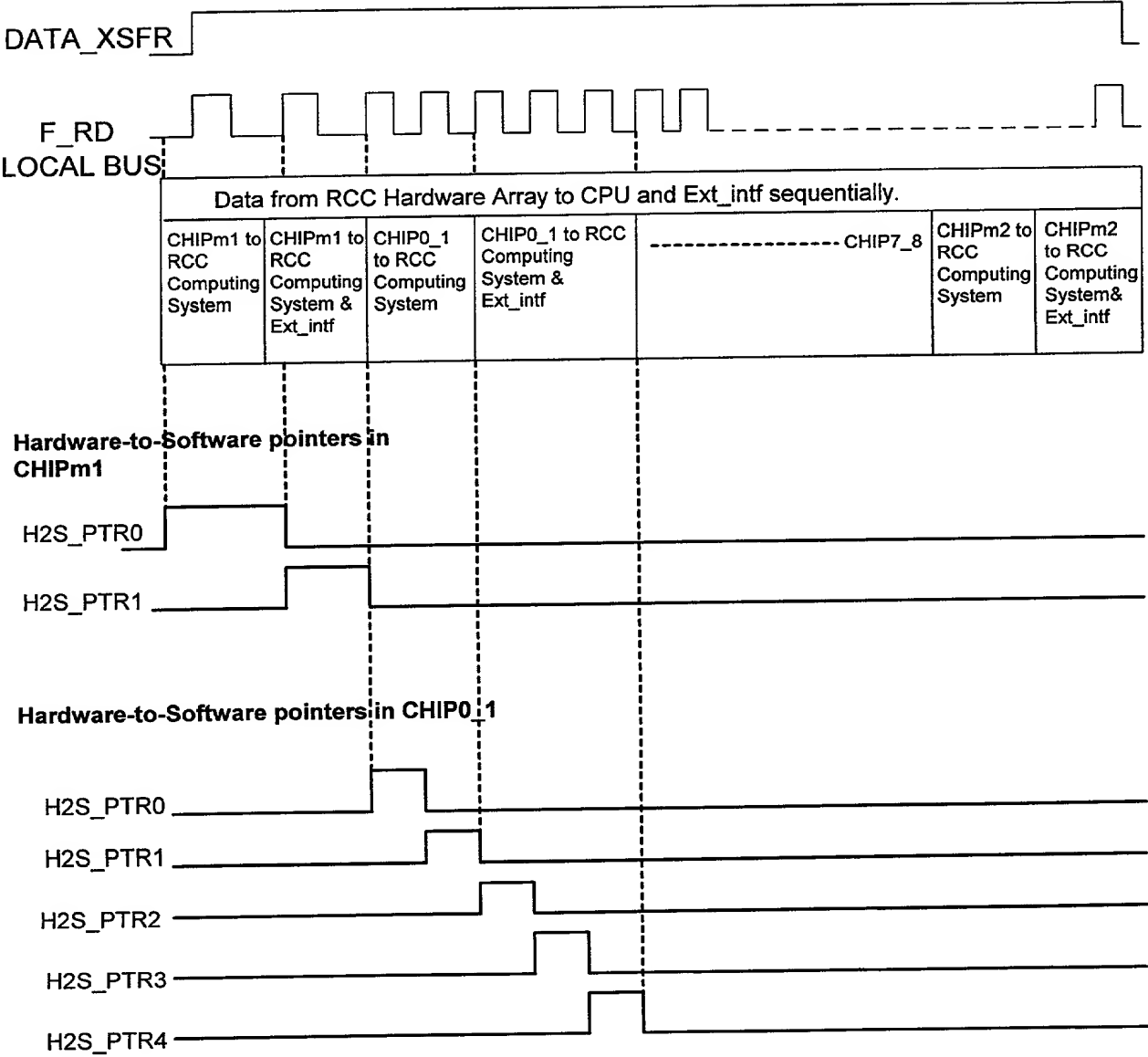


FIG. 73

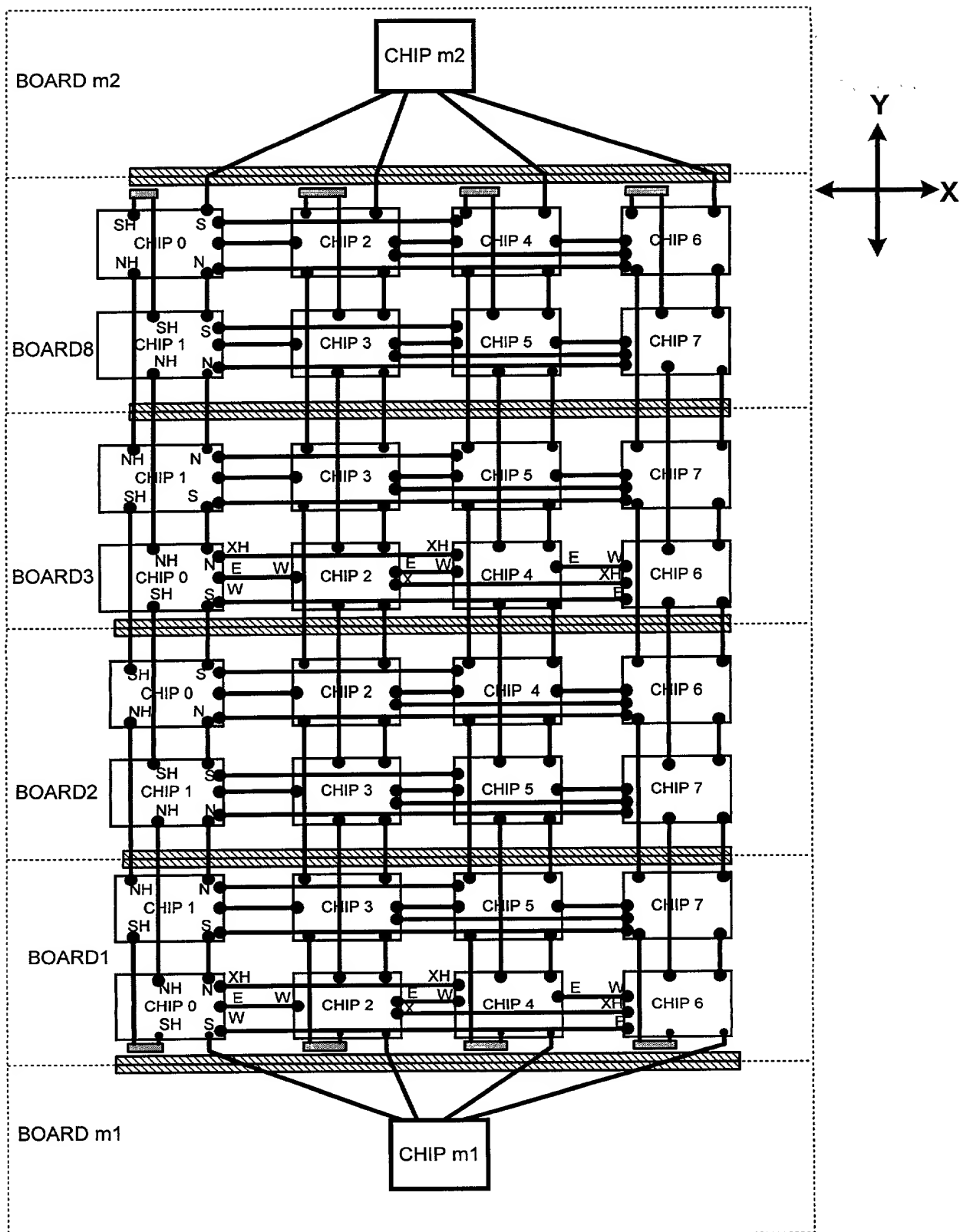


FIG. 74

Table 1. Demographic characteristics of the study population	
Age (years)	Mean (SD)
Male	55.2 (10.5)
Female	56.8 (11.2)
Marital status	
Married	78.5%
Single	21.5%
Education level	
High school or above	65.2%
Below high school	34.8%
Occupation	
White collar	45.1%
Blue collar	54.9%
Income (USD/month)	
< 1000	12.3%
1000-2000	35.7%
2000-3000	28.9%
> 3000	23.1%
Health insurance	
Yes	89.4%
No	10.6%
Comorbidities	
Hypertension	42.1%
Diabetes	18.5%
Cholesterol	31.2%
Smoking status	
Current smoker	15.3%
Former smoker	22.7%
Non-smoker	62.0%

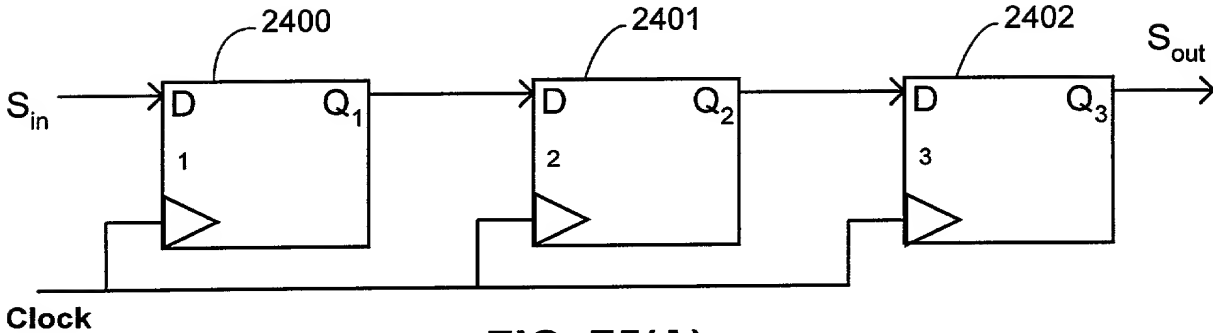


FIG. 75(A)

HOLD TIME ASSUMPTION FOR SHIFT REGISTER

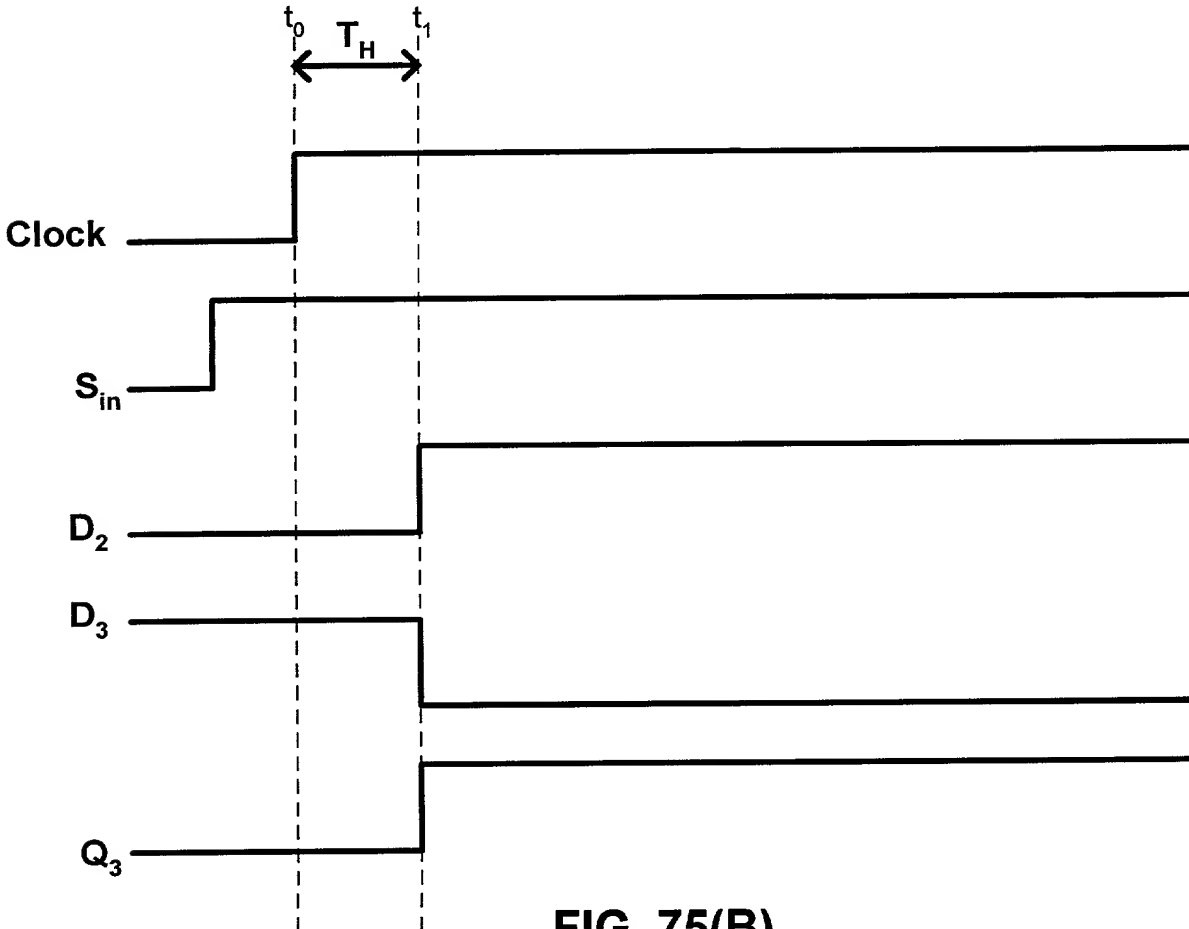


FIG. 75(B)

MULTIPLE FPGA MAPPING FOR SHIFT REGISTER

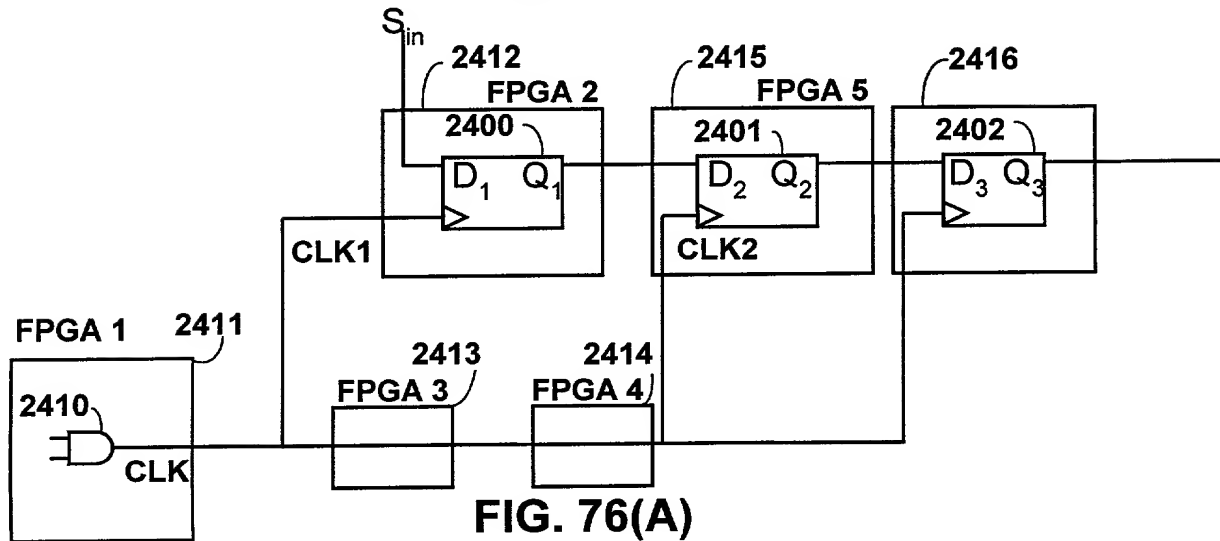


FIG. 76(A)

HOLD TIME VIOLATION BY LONG CLOCK SKEW

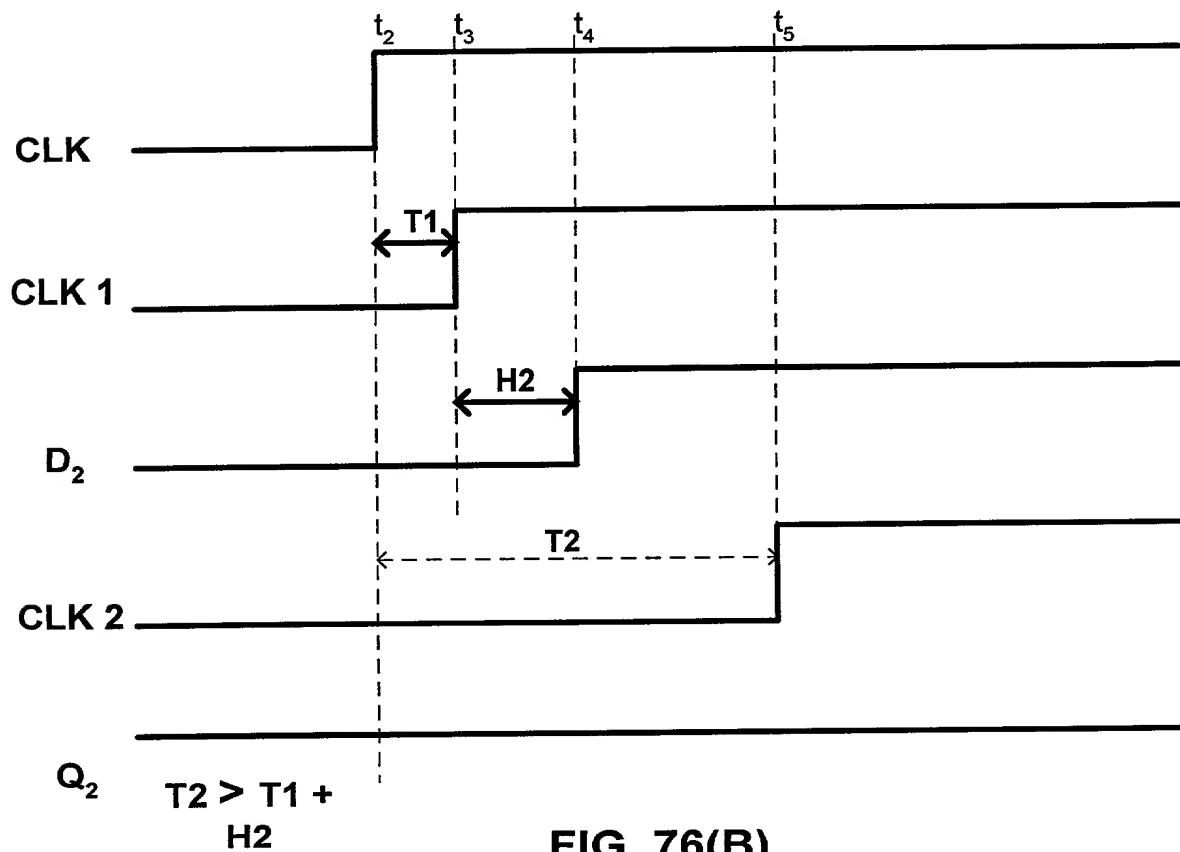


FIG. 76(B)

CLOCK GLITCH PROBLEM

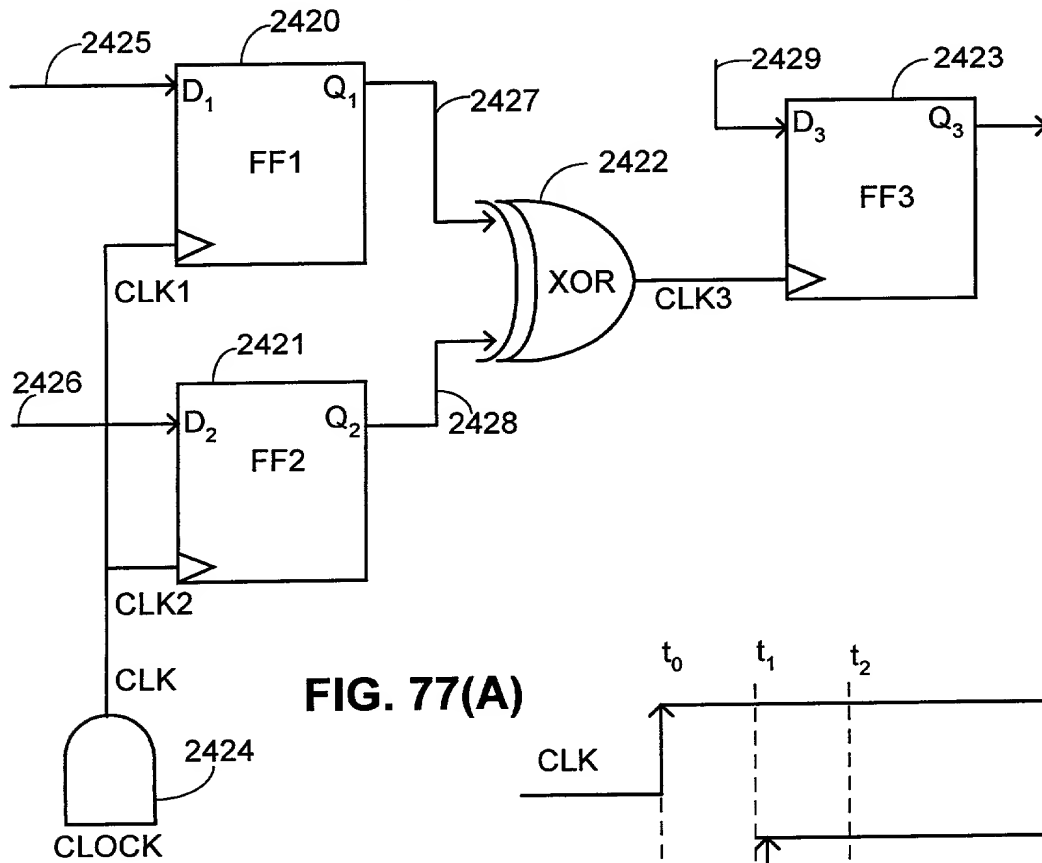


FIG. 77(A)

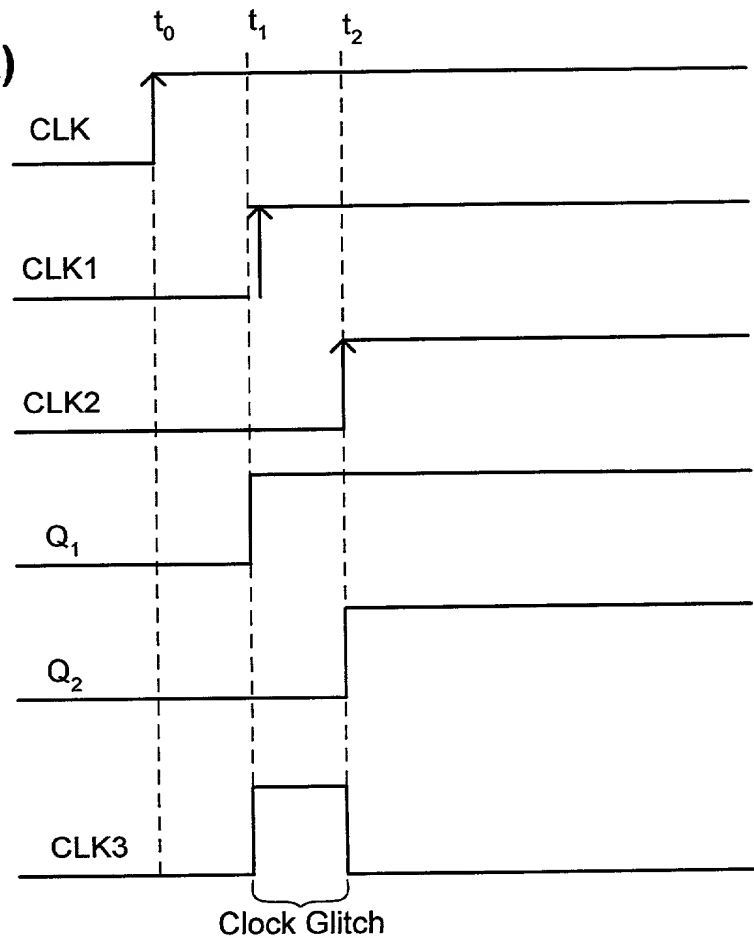
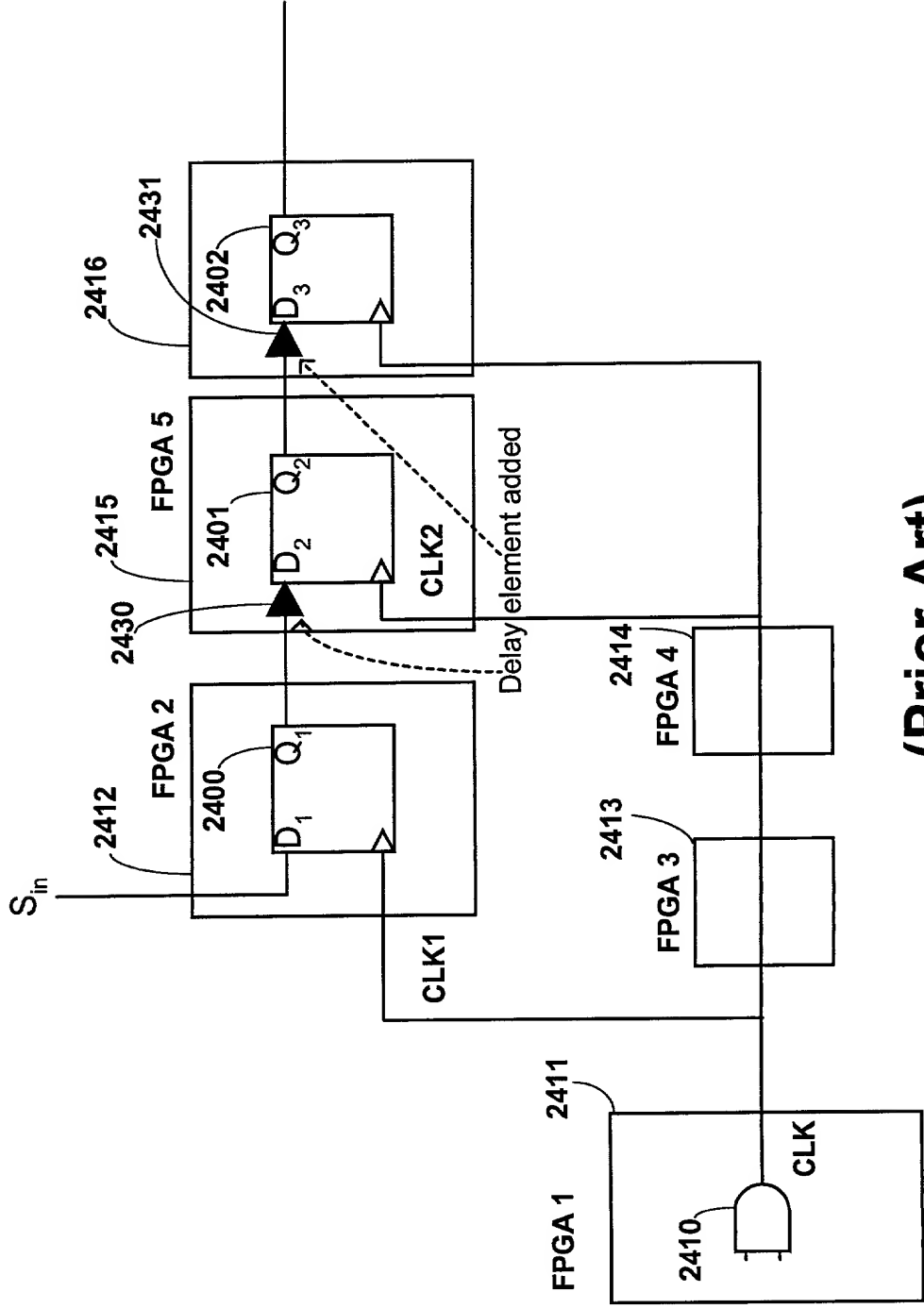


FIG. 77(B)

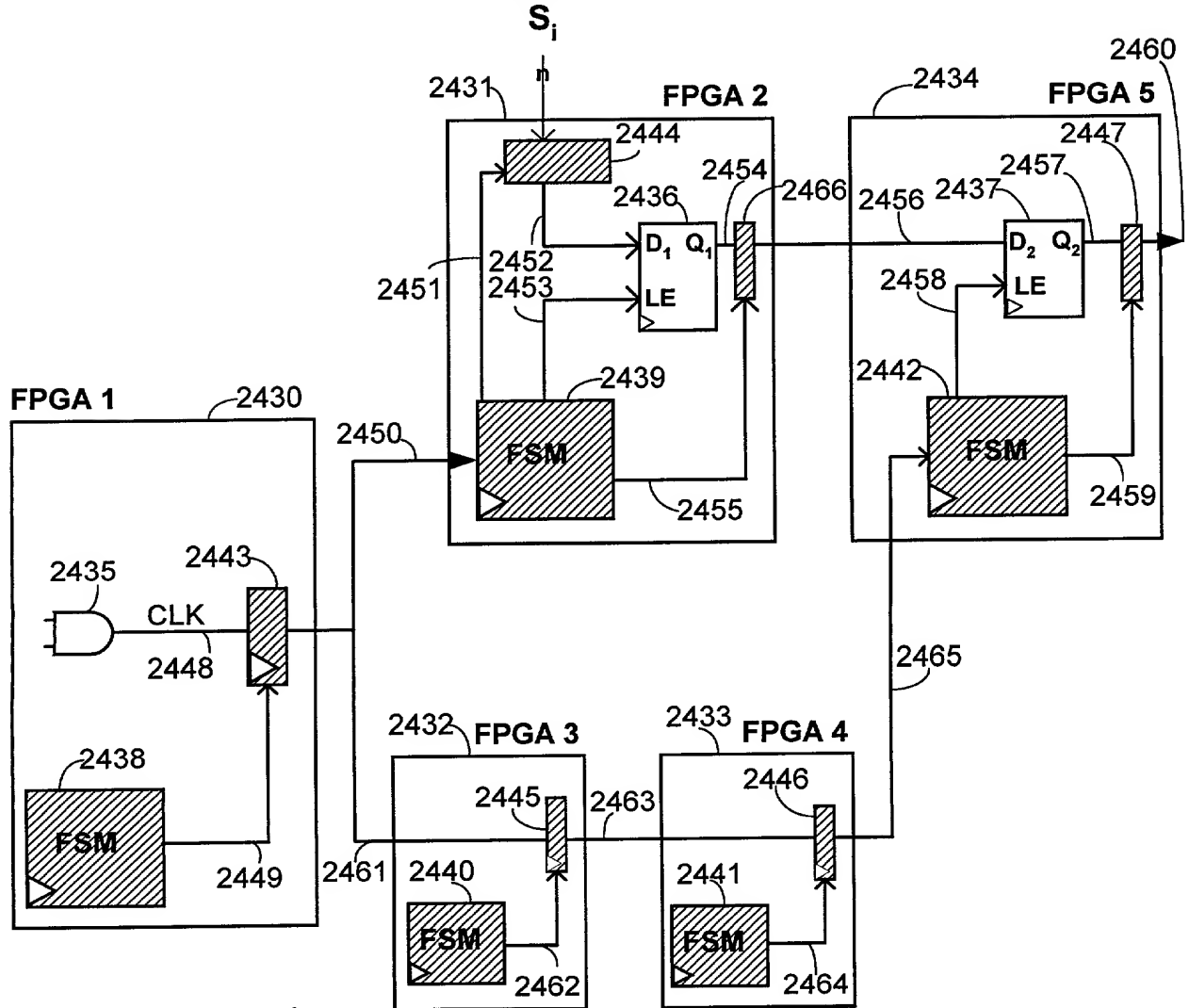
TIMING ADJUSTMENT BY ADDING DELAY



(Prior Art)

FIG. 78

GLOBAL RETIMING



Legend



Controlled by the global reference clock.



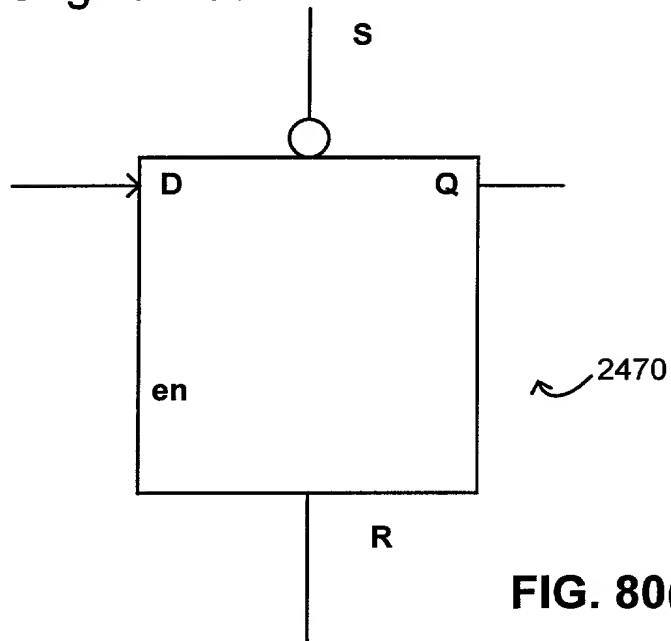
FSM and I/O registers for retiming control.

(Prior Art)

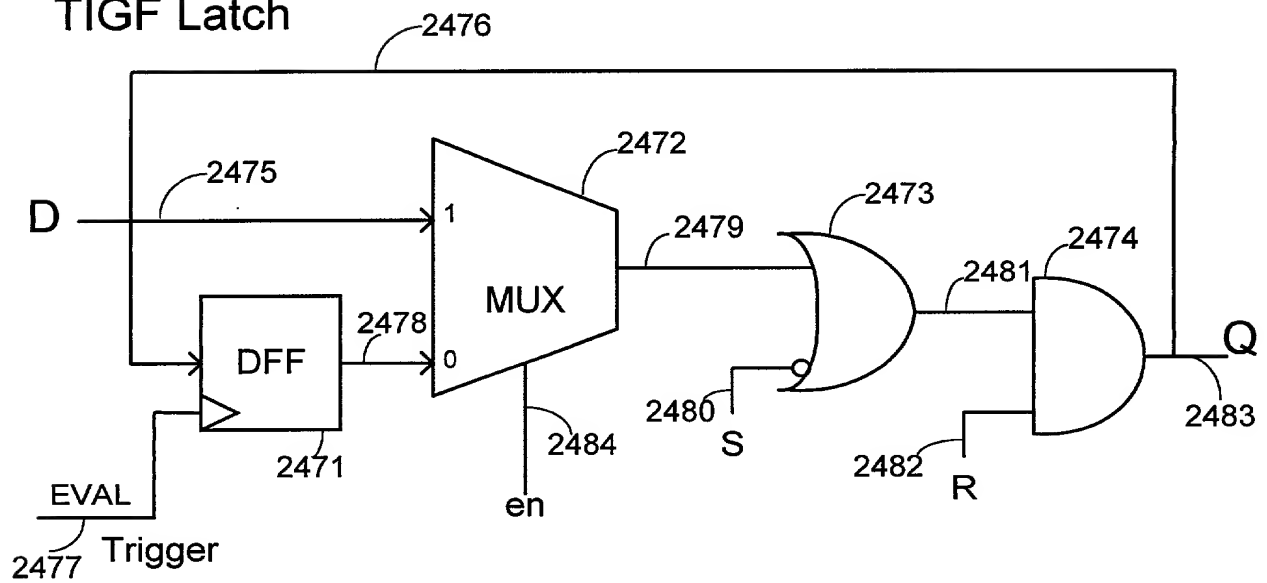
FIG. 79

TIGF LATCH

Original Latch



TIGF Latch



TIGF DFF

Original DFF

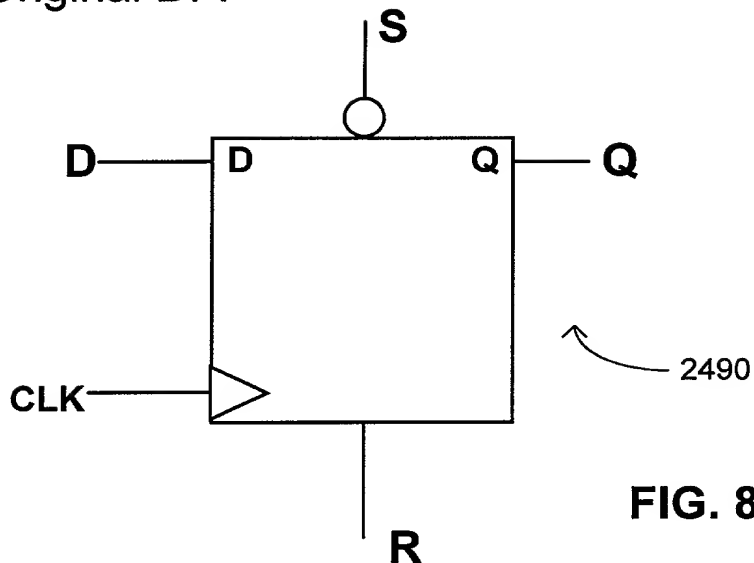


FIG. 81(A)

TIGF DFF and Edge Detector

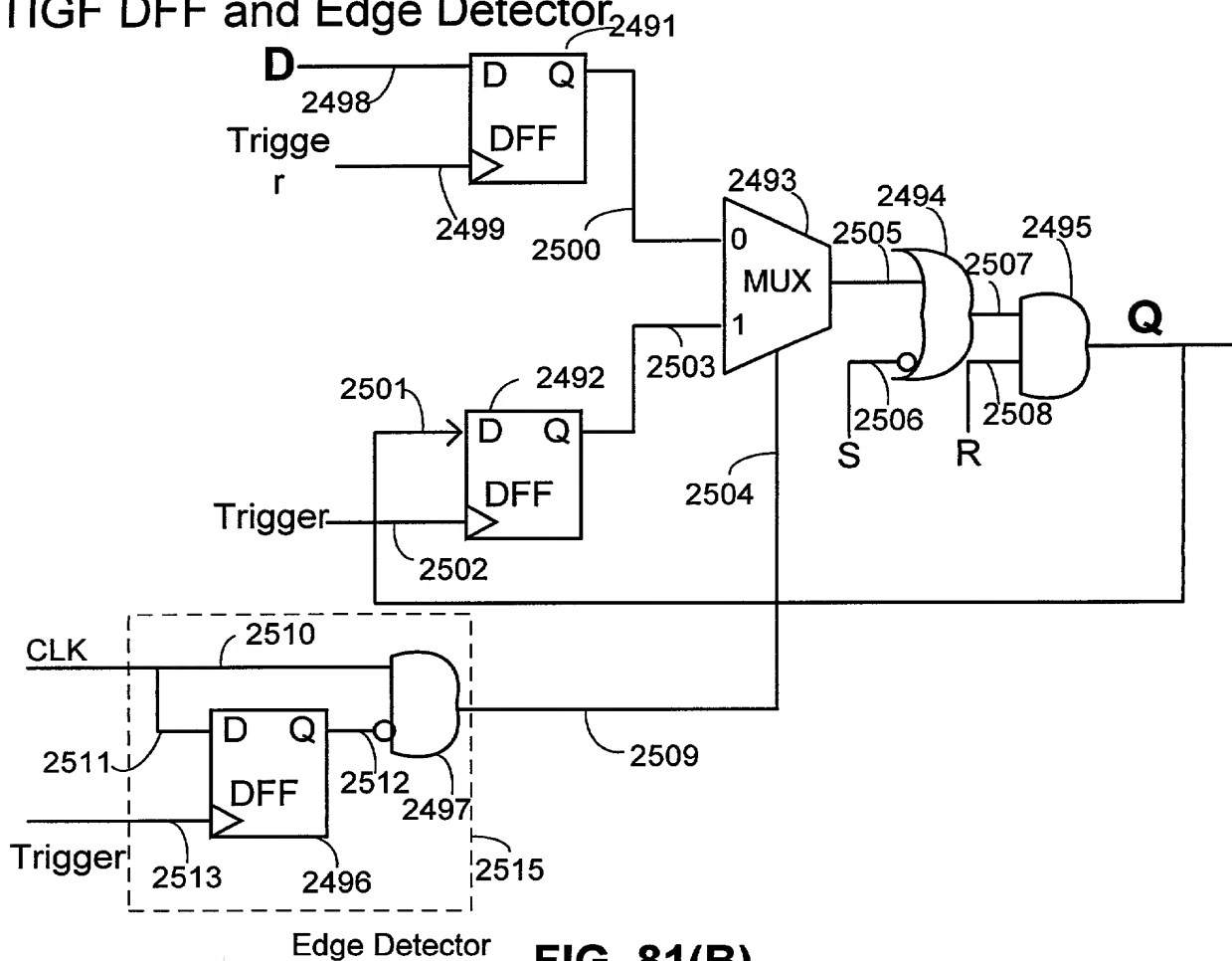


FIG. 81(B)

GLOBAL TRIGGER SIGNAL

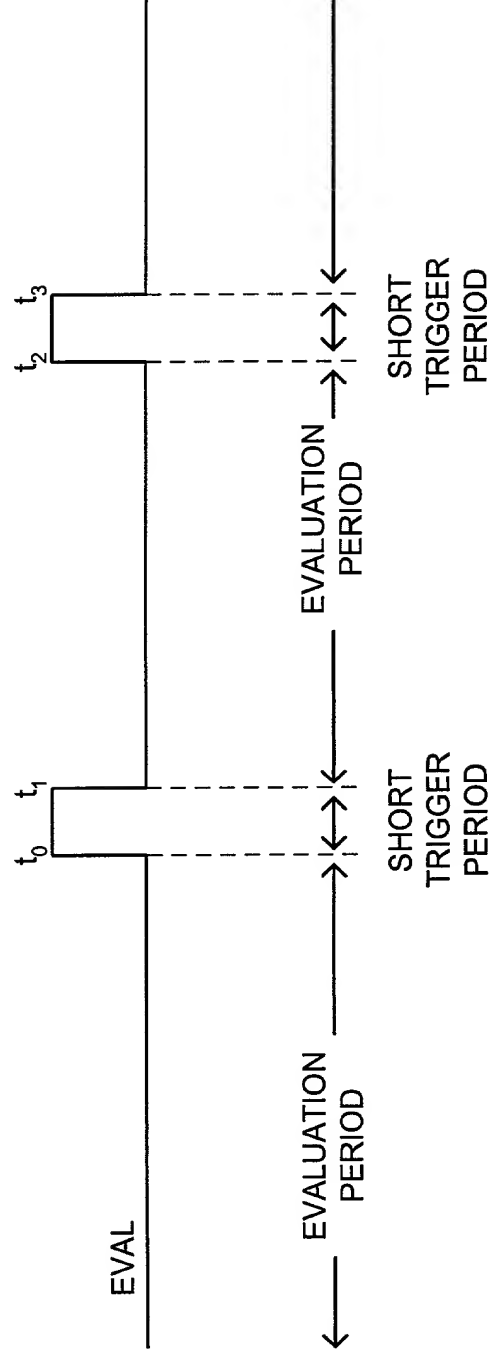


FIG. 82

RCC System

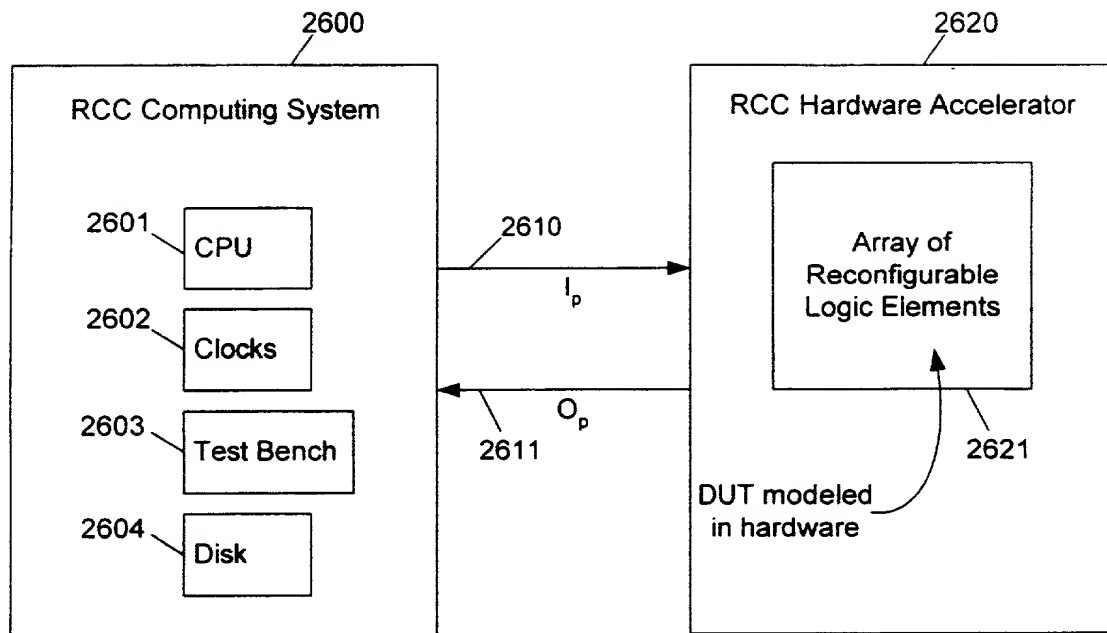


FIG. 83

FIG. 84

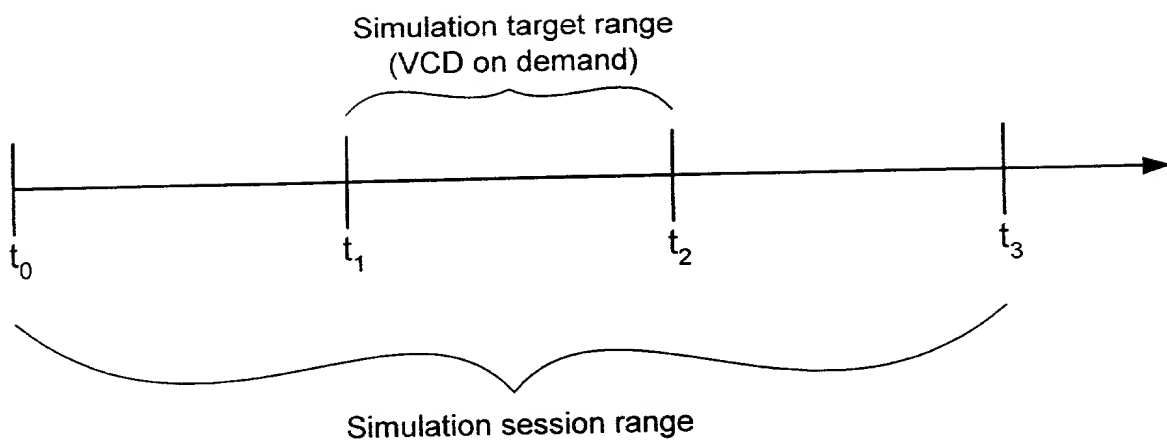


FIG. 84

SINGLE-ROW FPGA PER BOARD

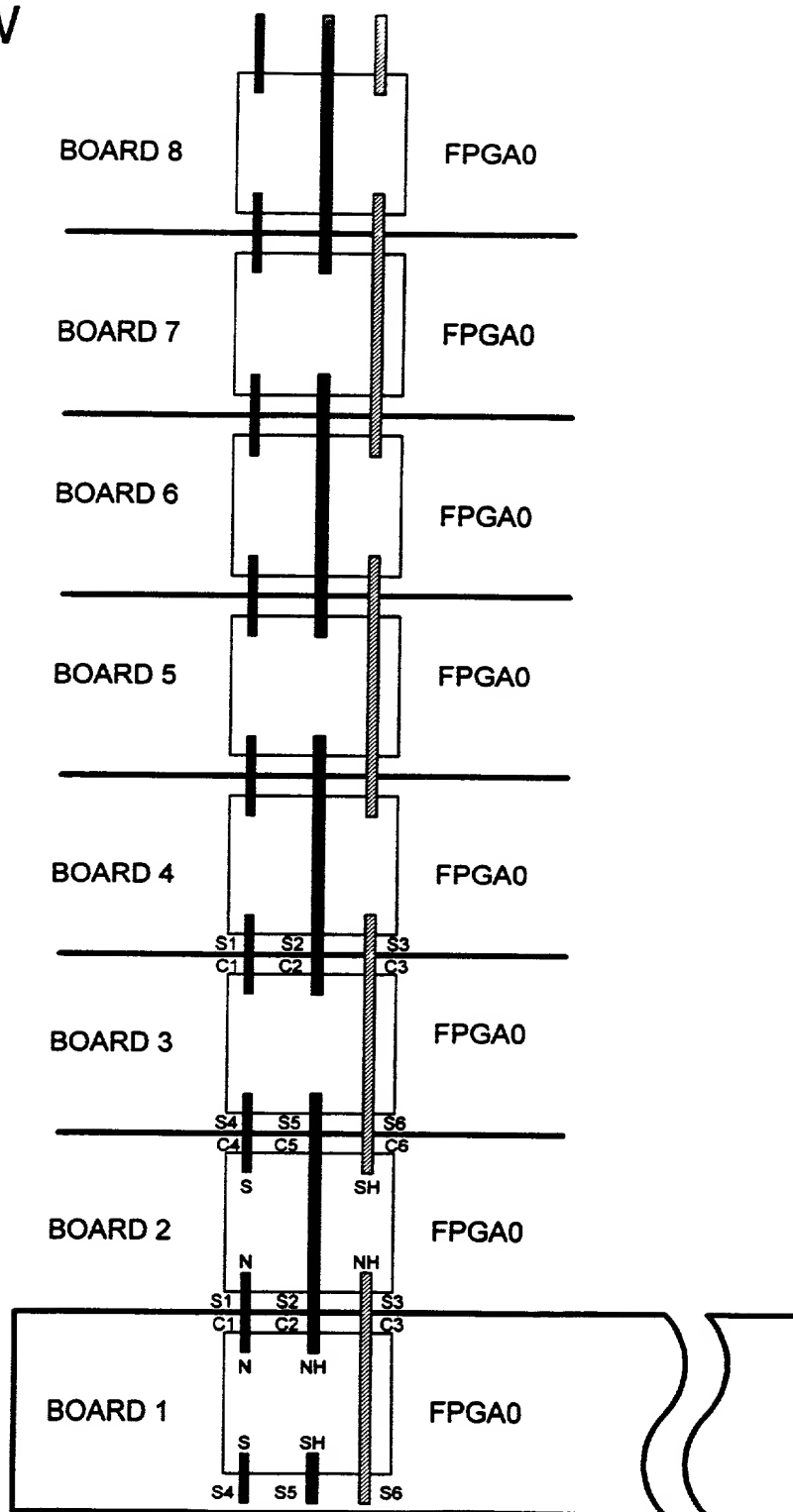


FIG. 85

TWO-ROW FPGA PER BOARD

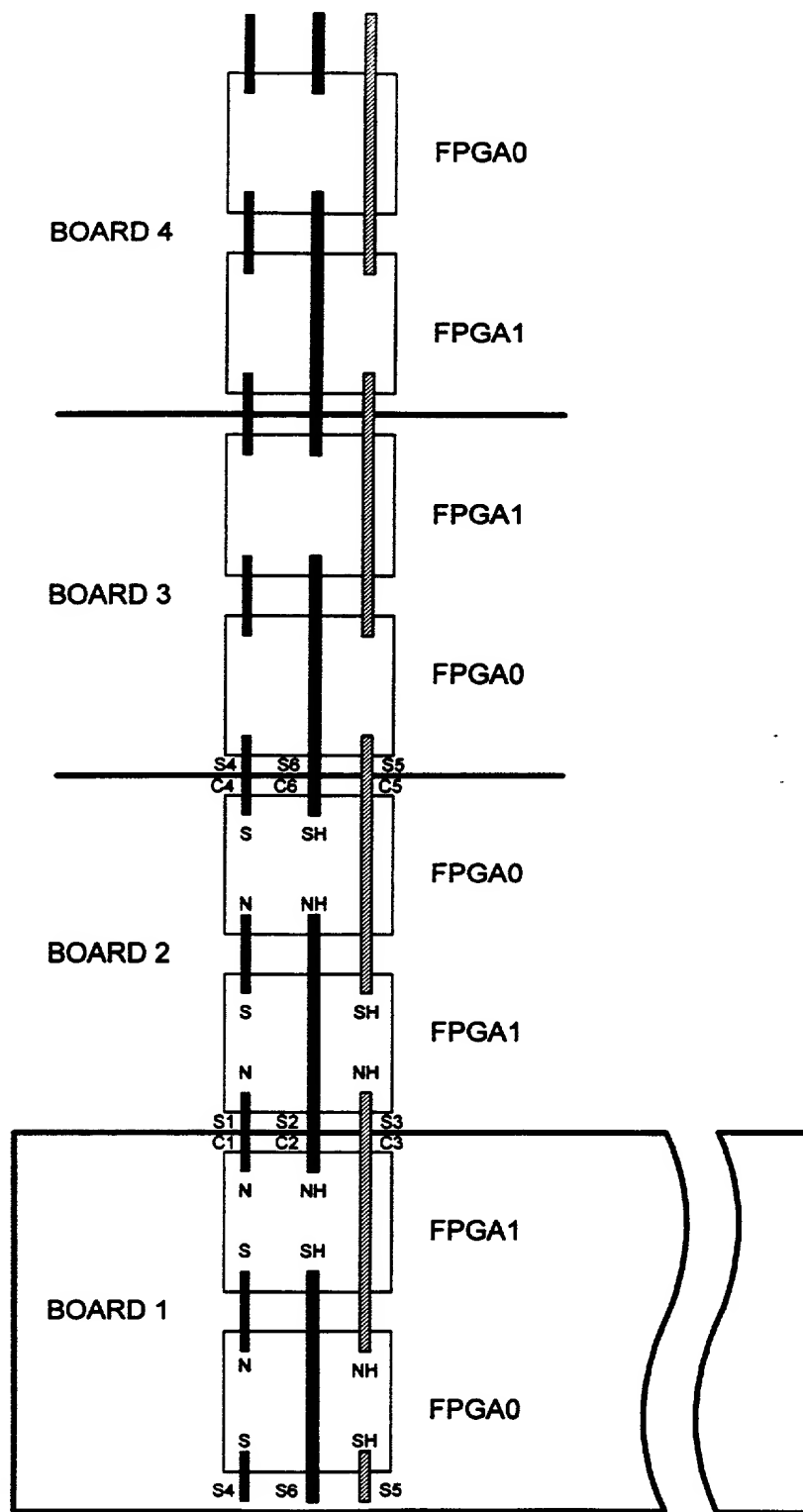


FIG. 86

THREE-ROW FPGA PER BOARD

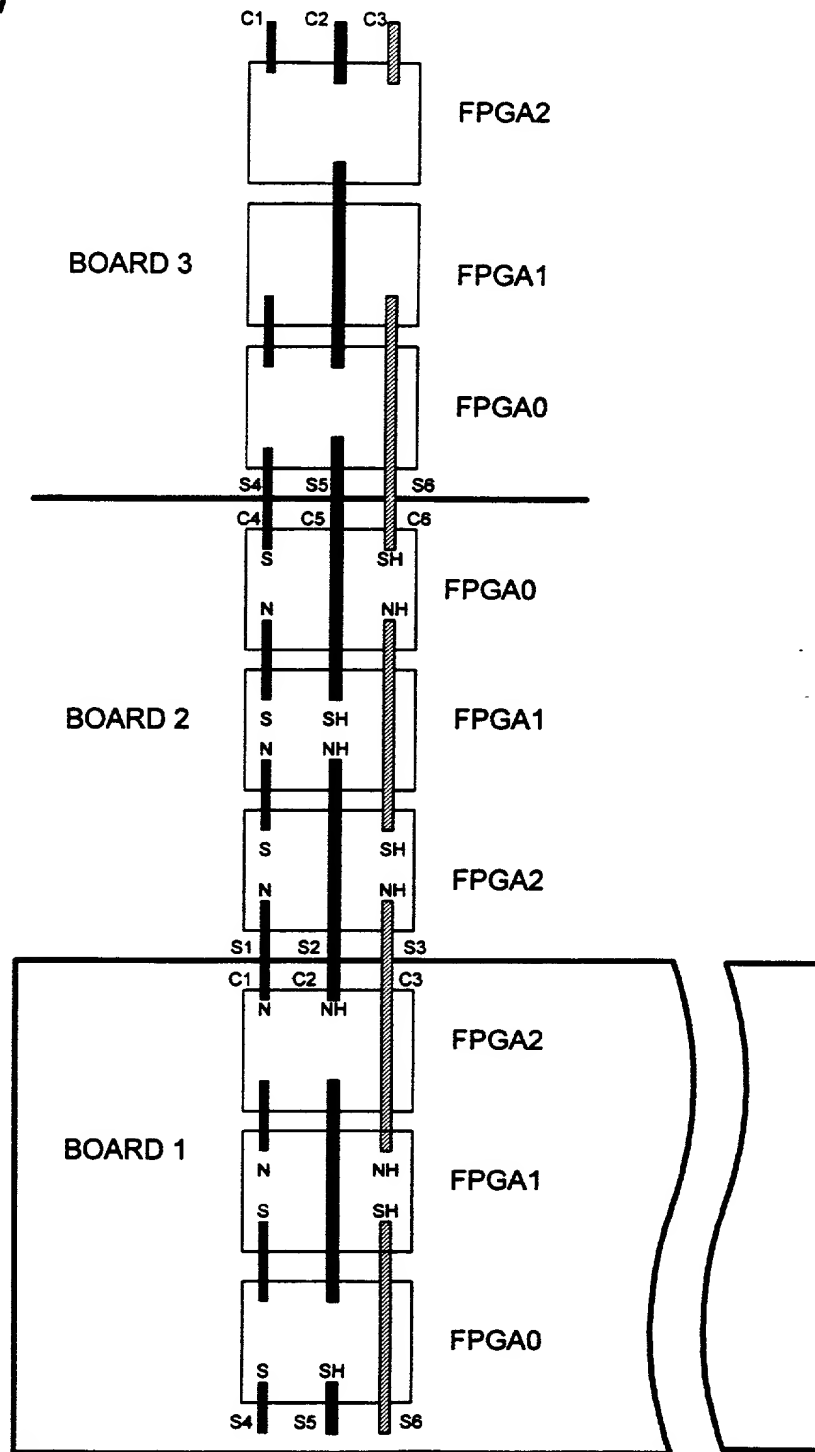


FIG. 87

FOUR-ROW
FPGA PER
BOARD

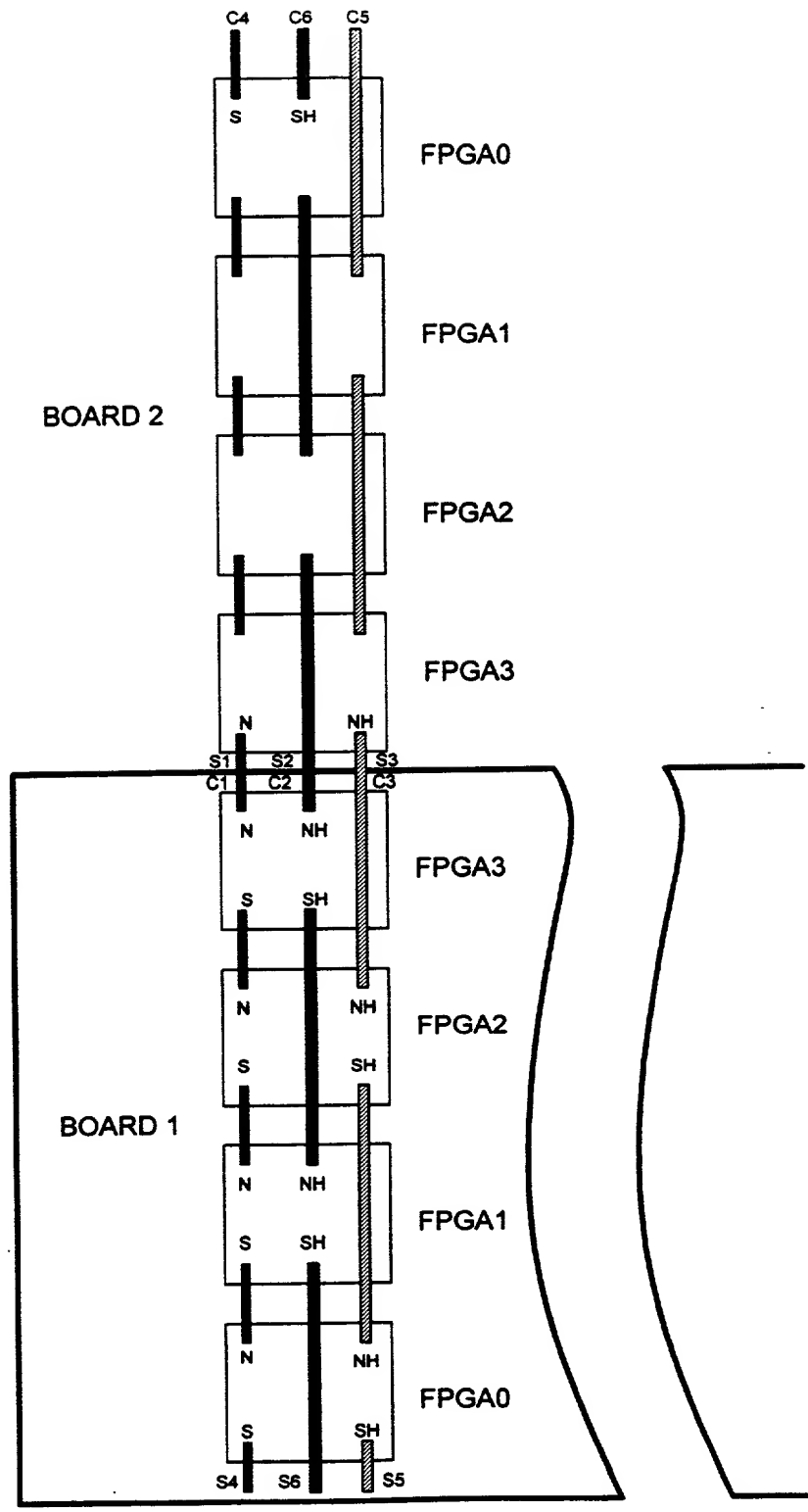


FIG. 88

INTERCONNECT FOR THREE-ROW PER BOARD

I/O Signals	Odd Board	Even Board	Common Board
	Connector-Group Pin-position	Connector-Group Pin-position	Connector-Group Pin-position
FPGA2_N	C1	S1	C1, S1
FPGA2_NH	C2	S3	C2, S3
FPGA1_NH	C3	S2	C3, S2
FPGA0_S	S4	C4	C4, S4
FPGA0_SH	S5	C6	C6, S5
FPGA1_SH	S6	C5	C5, S6

FIG. 89

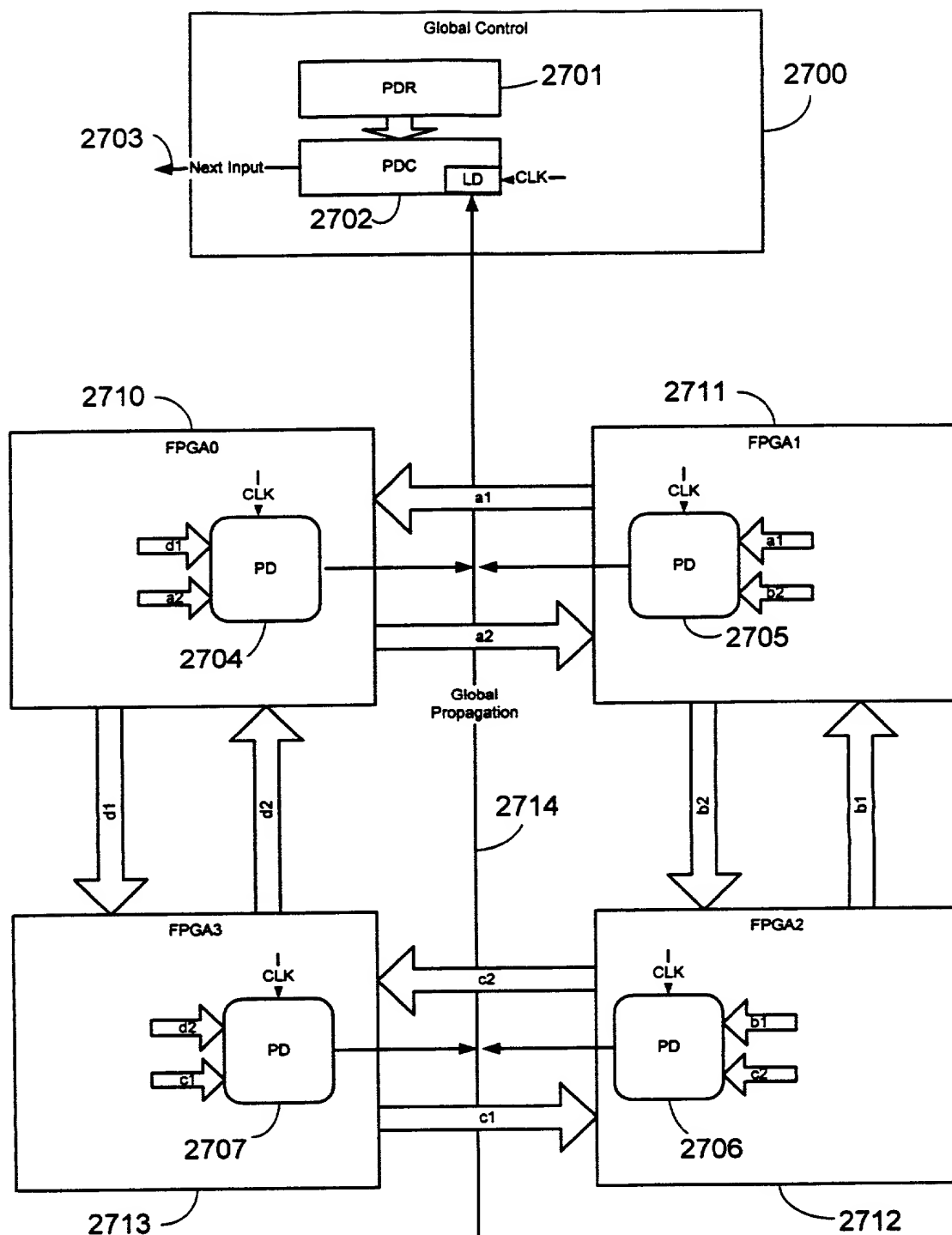


FIG. 90

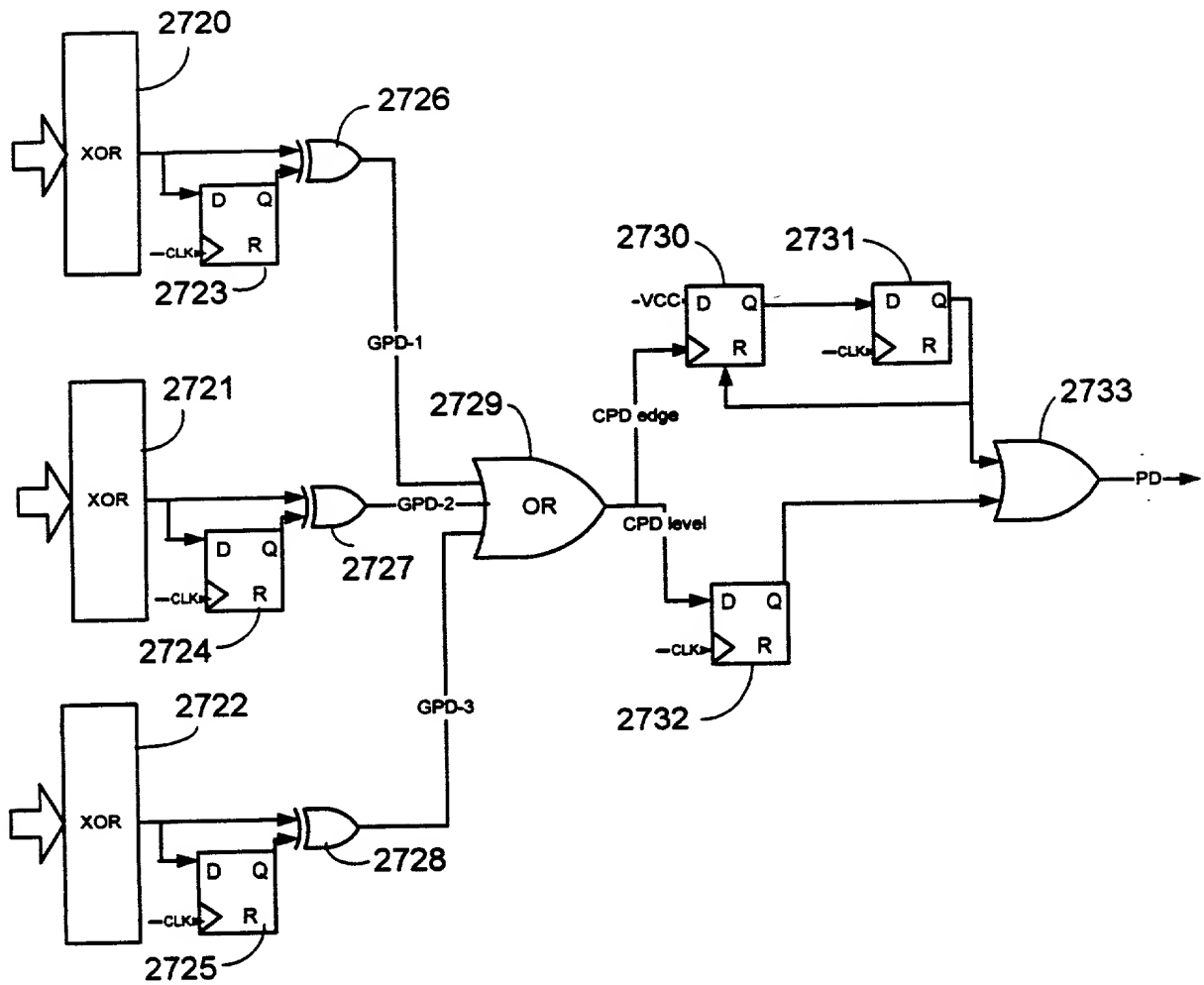


FIG. 91

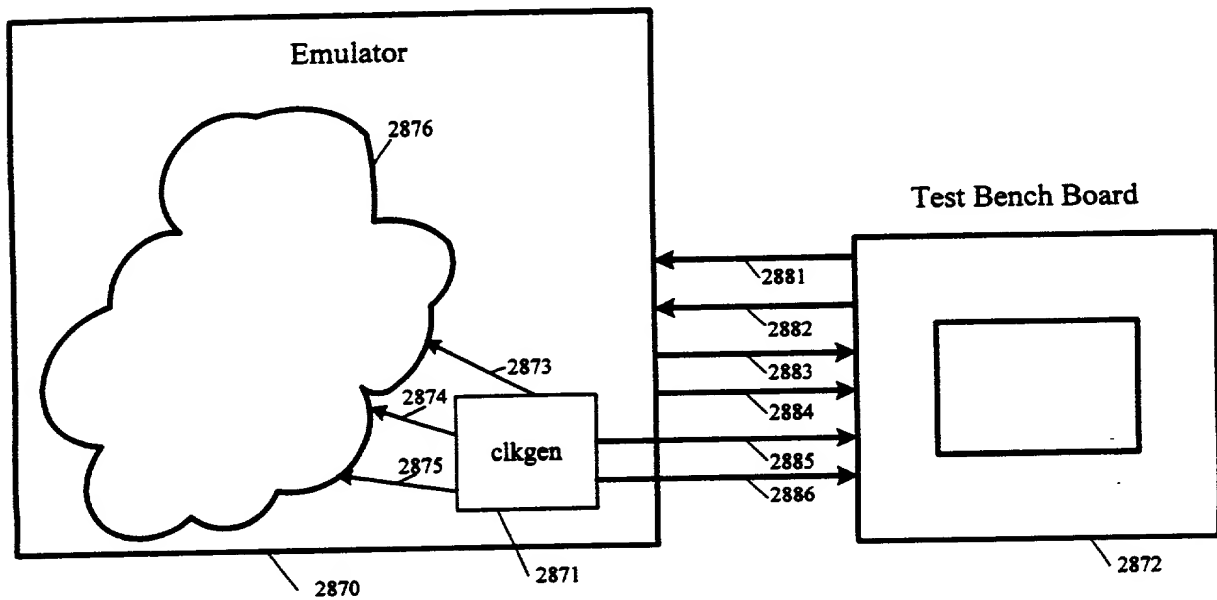


FIG. 92

Clock Specification

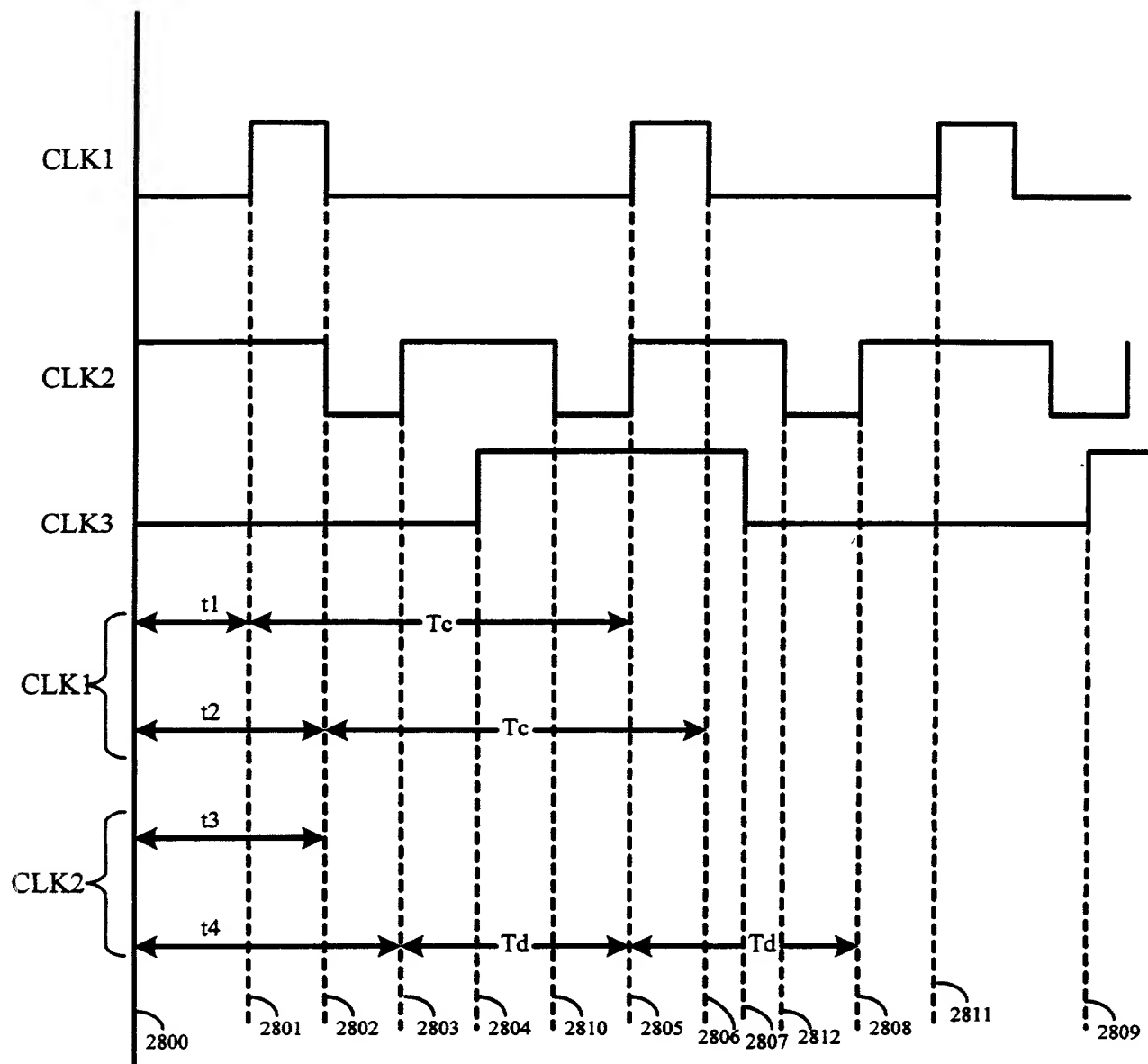


FIG. 93

Clock Generation Scheduler w/ Slices

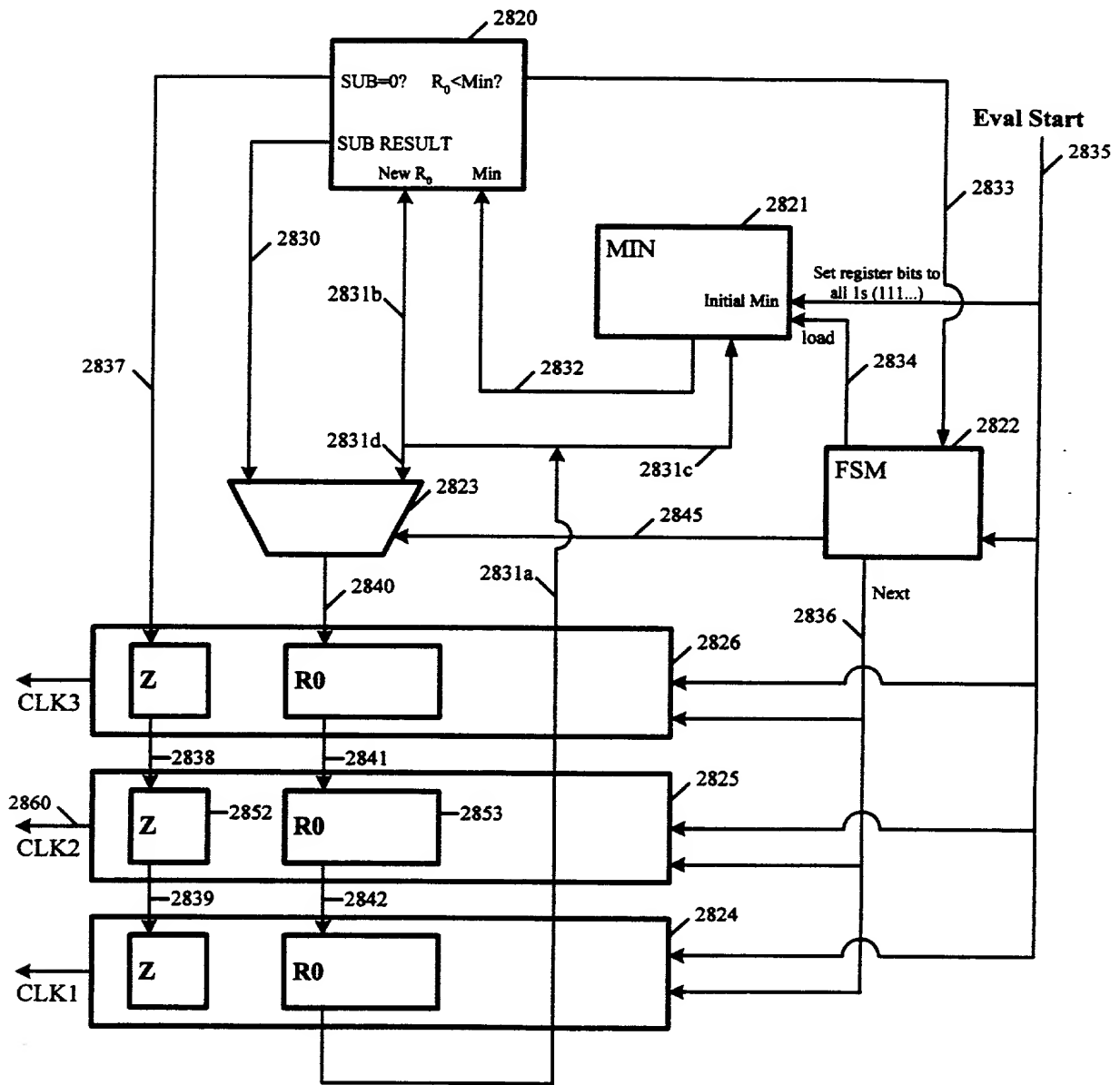


FIG. 94

Clock Generation Slice

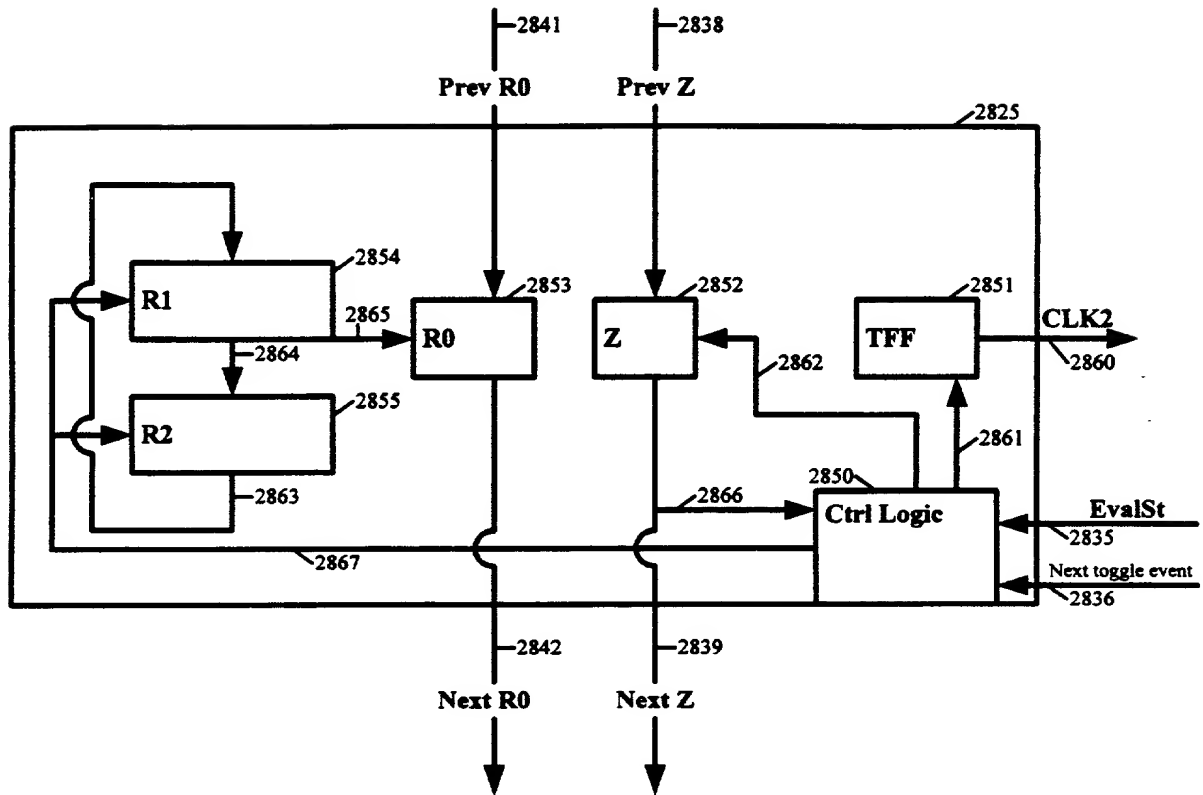


FIG. 95

Clock Generation Scheduler and Slices

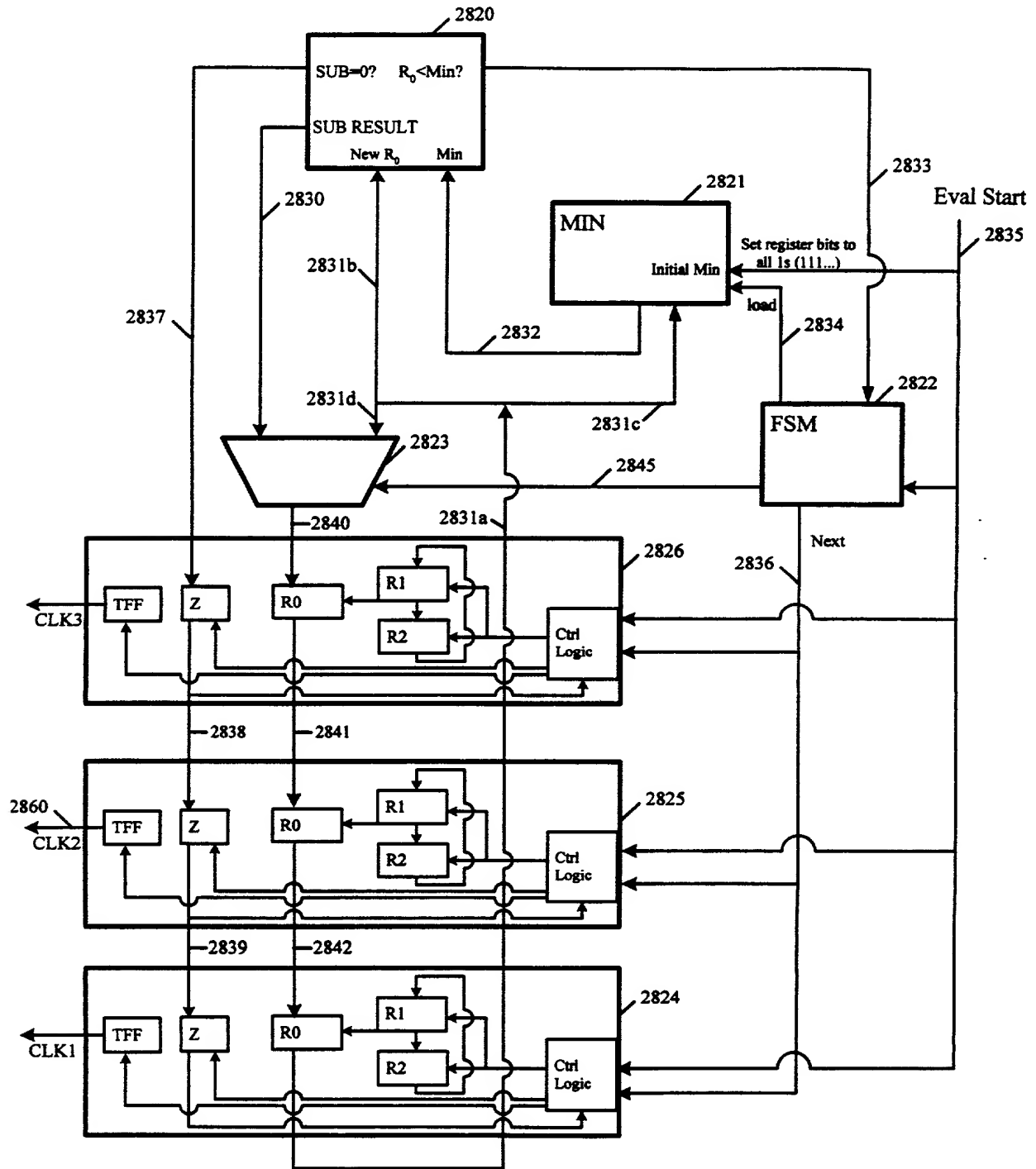


FIG. 96

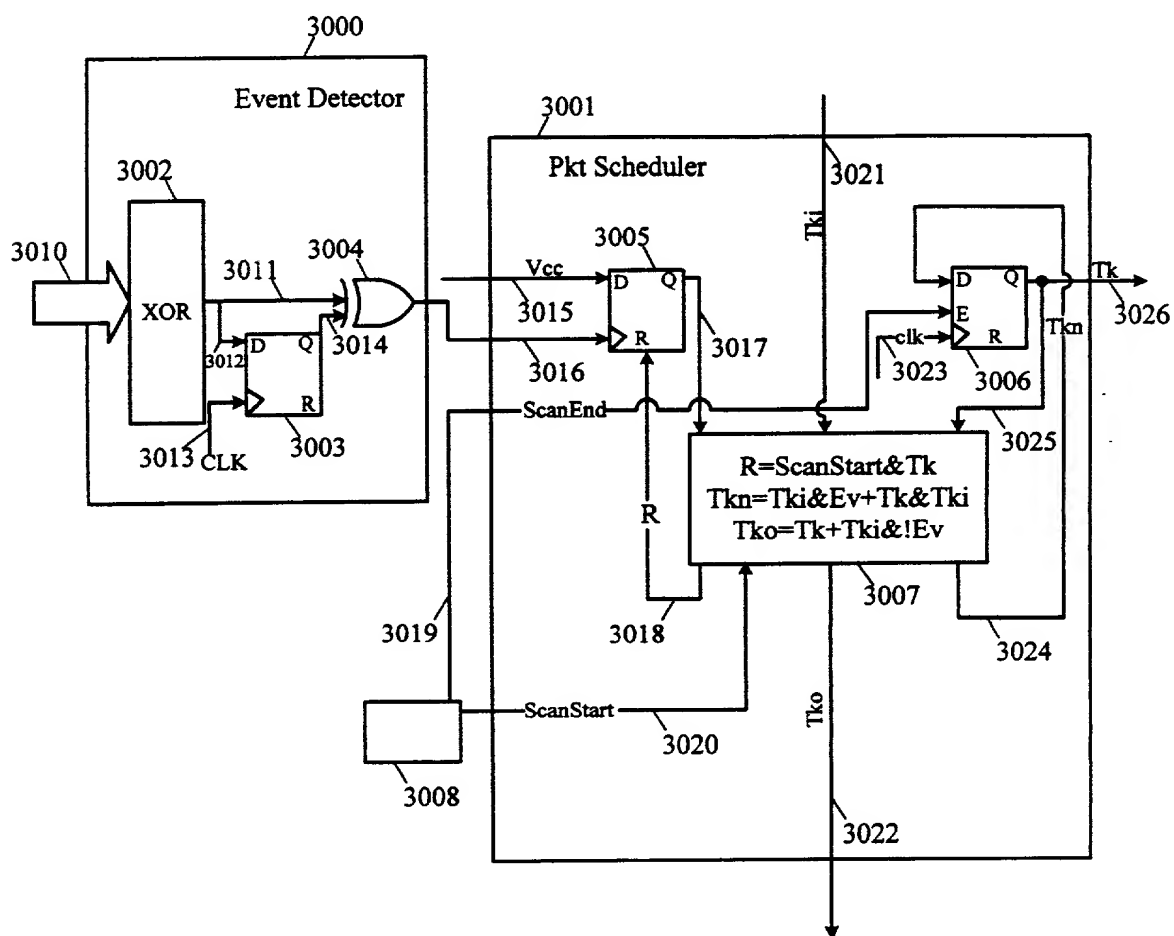


FIG. 97

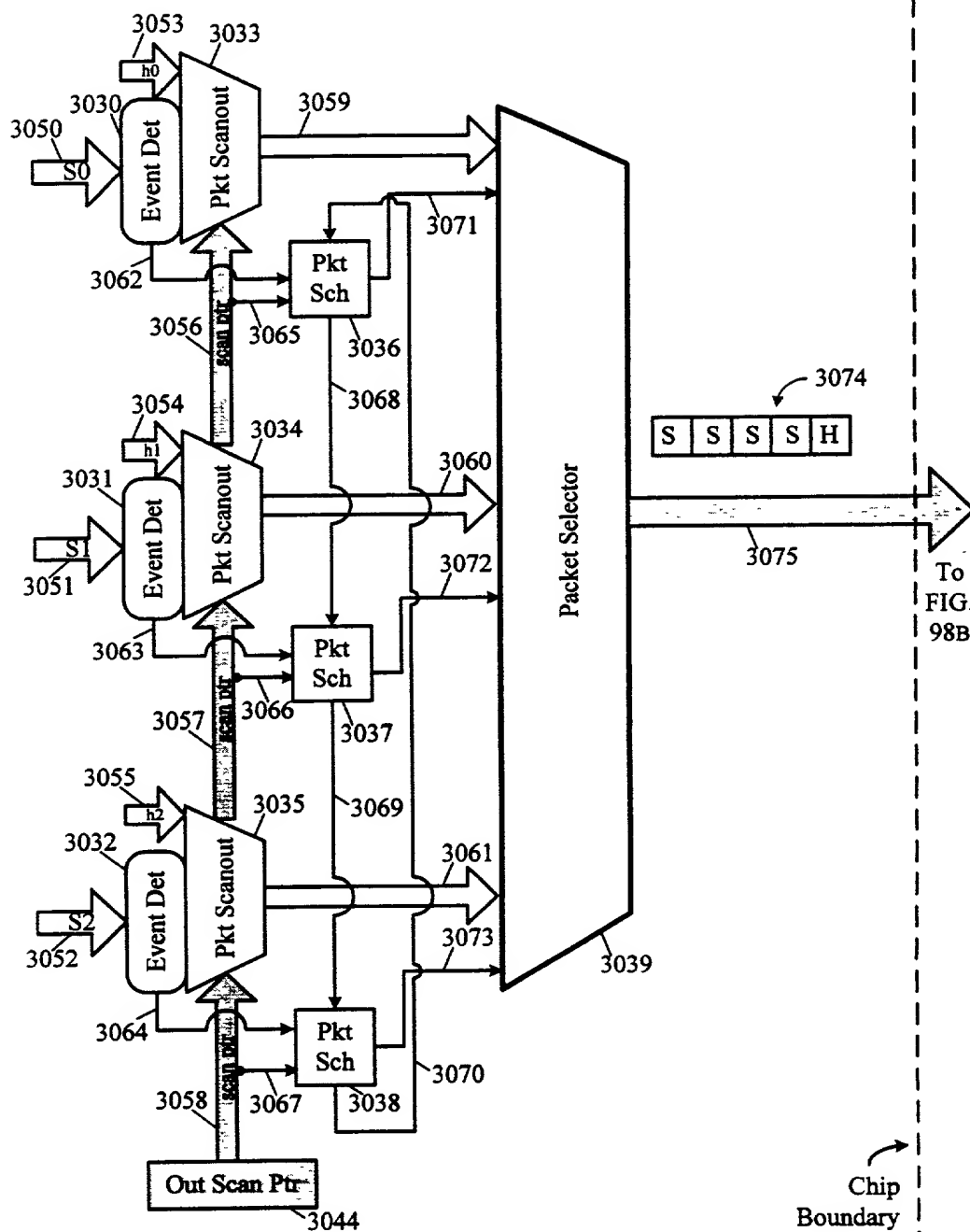


FIG. 98A

FIG. 98B

